High Efficiency Three Phase Nine Level Diode Clamped Multilevel Inverter

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Abstract: Nowadays the demand for DC-DC converters and related semiconductor components is an emerging expectation to meet the pursuit of energy efficiency and to reduce the power demand. Hence the Multiphase DC-DC converters based topology applied for high-voltage and high-power applications are proposed in this paper. The proposed converter is configured such that the boost - half-bridge (BHB) cells and voltage doublers are connected in parallel and in series to increase the output voltage and the output power. In addition, the proposed converter has the advantages of high-step-up voltage gain with significantly reduced transformer turn ratio, low input current ripple due to interleaving effect, zero-voltage switching turn-on of switches and zero-current switching turn-off of diodes, no additional clamping and start-up circuits required, high component availability and easy thermal distribution due to the use of multiple small components and flexibility in device selection results in better design. The inverter is capable of producing seven levels of output-voltage levels from the dc supply voltage. Multilevel inverters offer improved output waveforms and lower THD. A PWM switching scheme for the multilevel inverter is generally preferred. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The device current rating of the proposed multiphase converter is reduced by increasing the number of series connection.

Keywords: Diode Clamped Multilevel Inverter (DCMLI), DC-DC converter, pulse width modulation, zero current switching.

1. Introduction

Application of multilevel voltage source converter (VSC) is becoming popular in power and energy systems as results of its high power density, excellent performance and high reliability. Some of the conventional and emerging applications of VSC include flexible AC transmission system (FACTS), custom power devices and distributed energy system (e.g. Photovoltaic, Wind, Micro turbine) in transmission and distribution systems, respectively .The application of VSC in custom power devices and distributed energy system are the recent developments that going to change the entire distribution system in many ways. Custom power devices are introduced in the distribution system to deal with various power quality problems faced by industrial and commercial customers due to increase in sensitive loads such as computer and adjustable speed drives and use of programmable logic control in the industrial process [1]-[3]. These power quality problems could range from simple flicker to long duration power interruptions. When the problems occur the associated costs, including downtime, defects, and loss of production, can be substantial. Among various power quality problems, voltage sags are more serious as they can cause customer equipment to malfunction or a production shutdown. Voltage sags may be caused by remote faults, or change in loading conditions, such as motor starting and energizing capacitor or transformer .The voltage sags could Application of multilevel voltage source converter (VSC) is becoming popular in power and energy systems as results of its high power density, excellent

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As the durations of voltage sag are so short, conventional voltage control methods such as tap changing transformers or capacitors with controls are not effective. Fast, more flexible voltage control methods are needed and power electronic system based power semiconductor devices can be used. An effective way of controlling the sags is to inject

Volume 1 Issue 3, December 2012 www.ijsr.net power into the system using custom power devices. Ideally, the systematic power needed for voltage control could be synthesized using a voltage-sourced inverter with small reactive component. An inverter-based compensator could have higher performance, small size, lower cost, and lower harmonic than conventional topologies .However, the use of VSC in utility application has been limited because of the limited power rating of self commutated switches when used in two-level voltage source inverter. The multilevel VSC is proposed in recent years as they can avoid the power barrier by using a modular approach in which switching devices are stacked together, in almost an unlimited fashion. The number of inverter "voltage level" is proportional to the number of dc bus capacitor tap points .As more voltage levels are added to the inverter, the harmonic performance improves without increased switching losses. Hence, in this paper a multilevel VSC, namely diode clamped voltage source converter, is proposed for high voltage distribution system applications.

2. Multilevel VSC Topology

During the last 10 years, there has been steady growth multilevel converter topology as they can suit for the high voltage and high power applications. Multilevel VSC are the attractive technology for the medium voltage application, which includes power quality and power conditioning applications in the distribution system. The most well-known multilevel topologies developed so far are shown in Figure 1. These are diode clamped multilevel voltage source converter (DC-VSC). These multilevel topologies can generate multilevel output voltages with low harmonics.

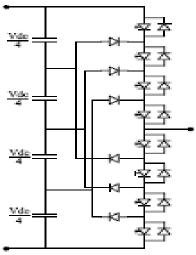


Figure 1: Multilevel VSC Topology

3. Diode-clamped multilevel inverter

An m-level diode-clamp inverter typically consists of m - 1 capacitors on the dc bus and produces m levels of the Phase voltage. A one leg of three-phase nine-level diode-clamped inverter is shown in Figure 3. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by eight capacitors into nine levels. The voltage across each capacitor is, and the voltage stress across each switching device is limited to the safe working level through the clamping diodes. Figure 2 shows one of the three line-line output voltage waveforms for a nine-level multilevel

inverter. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is a 9-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage.

Although each active switching device is required to block only a voltage level of dc V, the clamping diodes require different ratings for reverse voltage blocking.. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series; consequently, the number of diodes required for each phase would be 2(m-2). Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped inverter. DCMLI has the following advantages and disadvantages.

3.1 Merits

- DC-link capacitors are common to three phases.
- Switching frequency can be low.
- Reactive current and negative-phase sequence current can be controlled.

3.2 Demerits

- Many diodes are used for clamping.
- Many diodes make physical layout difficult e.g. increase stray inductance

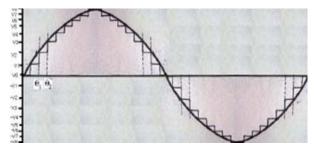


Figure 2: Output line Voltage of 9 levels DCMLI

4. PWM method for 9-level DCMLI

Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel inverters. Previous authors (McGrath, B.P. and D.G. Holmes) have extended several different two-level multilevel carrier-based PWM techniques as a means for controlling the active devices in a multilevel inverter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase [8]-[10]. Figure 4 shows the principle of the PWM method for a multilevel inverter. The PWM method generates switching signals by comparing one sinusoidal signal and eight triangular wave signals, which have DC bias for each voltage level, as shown in Figure 4. In this modulation method, the duty cycle of each voltage level is determined by the ratio of the 4 sine wave amplitude to the triangular carrier signal amplitude. That is, the sine wave amplitude determines modulation factor, and one modulation factor generates only one pattern of output pulse width. Using PWM modulation explained above, simulations have been conducted to verify the effectiveness of the algorithm. PWM modulation in MATLAB Simulink block diagrams and the nine-level DCMLI is shown in Figure.3

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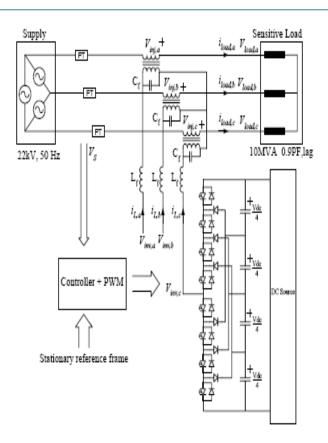


Figure 3: Three-phase nine-level diode-clamped inverter

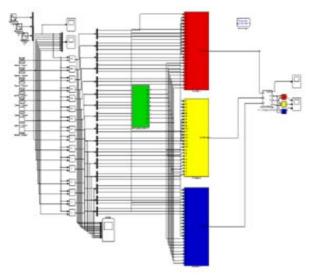


Figure 4: Nine-Level inverter Model

4. Simulation results

The gate signals of DCMLI power circuits are produced by triangle and sinusoidal comparison in MATLAB/Simulink blocks. The output of nine-level DCMLI is connected to a load and the voltage waveforms are shown in Figure 5. In order to get THD level of the waveform, a fast Fourier transform (FFT) is applied to obtain the spectrum of the output voltage, which is shown in Figures 5. The THD of the output voltage of nine-level DCMLI is 7.84% shown in Figure.7, which shows that lower order harmonics, have been eliminated. THD levels of seven levels DCMLI and nine levels DCMLI are compared in Table 1. From the table,

it is clear that the THD value of nine levels DCMLI is lower than that seven level DCMLI.

Table 1: THD of seven and nine level DCMLI

DCMLI	Seven Level	Nine Level
THD	10.47%	7.84%

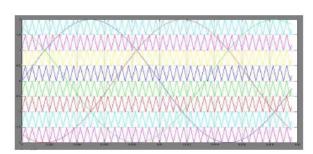


Figure 5: Sinusoidal PWM

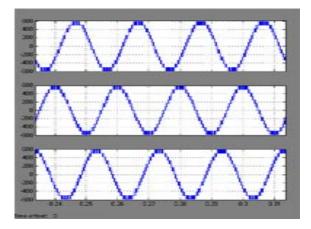


Figure 6: Simulation Nine Level Ouput Line Voltage

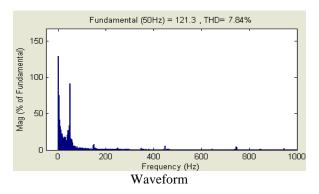


Figure 7: FFT Analysis of Nine Level Inverter

5. Conclusion

This paper presents a multilevel voltage source converter. As the ratings of various power electronic switches are limited, multilevel voltage source converter topologies are useful for high voltage and high power applications along with low harmonics. Diode-Clamped multilevel voltage source converter is selected for DVR application as the number of capacitors needed and switching states are less compared to other topologies. The nine-level diode-clamped multilevel inverters for harmonic elimination in MATLAB/ Simulink software package have been presented. The THD levels of

Volume 1 Issue 3, December 2012 www.ijsr.net seven levels DCMLI and nine levels DCMLI are compared. Simulation results reveal that the THD of nine levels DCMLI is less than the seven levels DCMLI. Therefore it is concluded that the THD will be decreased by increasing the level of DCMLI.

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