

Fault Detection and Classification in Transmission Line Using FPGA

Sumit S. Chincholkar¹, Dr. S. A. Naveed²

¹PG Student, BAMU University, MGMs J.N.E.C, Aurangabad, Maharashtra, India

²Professor, BAMU University, MGMs J.N.E.C, Aurangabad, Maharashtra, India

Abstract: *This paper presents a hardware efficient logic for fault detection and classification in transmission line using wavelet transformation technique, kNN algorithm and implemented using a field-programmable gate array (FPGA). The general SPARTAN3E FPGA board was employed for prototype development. All the coding done by using hardware description language called very high speed integrated circuit (VHDL). The alternating current signal samples are inputs to the system and is based on wavelet analysis. Since fault is associated with high frequency transients from current signals, depending on amount of high frequency components in current signals the faults are classified. MATLAB was used to apply the current signal input samples to the prototype. An adaptive threshold technology was used rather than fixed threshold in order to make classification more accurate and reliable using k NN algorithm or Standard deviation technique. The output of the proposed logic was shown in MODEL-SIM Software. A high level of computational efficiency is achieved in this algorithm as compared to the other wavelet based algorithms as only the high frequency details at first level are employed.*

Keywords: Fault Classification, Fault detection, Field programmable gate array (FPGA), transmission line, Wavelet transform

1. Introduction

Transmission lines constitute the major part of power system. Transmission and distribution lines are vital links between the generating unit and consumers to achieve the continuity of electric supply. Transmission lines also form a link in interconnected system operation for bi-directional flow of power. Transmission lines run over hundreds of kilometers to supply electrical power to the consumers. They are exposed to atmosphere, hence chances of occurrence of fault in transmission line is very high which has to be immediately taken care of in order to minimize damage caused by it. It will also facilitate quicker repair, improve system availability and performance, reduce operating cost and save time and effort of maintenance crew searching in, sometimes in harsh environmental conditions. Conventionally, fault detection and classification were achieved based on impedance calculations using power frequency voltages and currents. The accuracy of such methods depends on the performance of voltage and current measurement/estimation techniques. The complexity of the task is further aggravated by the involvement of random variation in several parameters like fault type, location, angle of incidence, fault impedance etc. A number of knowledge/expert/fuzzy- and artificial-neural-network-based techniques for fault classification are reported in literature [1]–[4]. The main requirement here is the availability of past system data and expert knowledge of the field engineers and, hence, is system dependent. Traveling-wave-theory-based fault classification schemes were also employed [5] but are rather computationally intensive.

In the field of signal processing we have different techniques, amongst that wavelet transformation is an important tool for high frequency transient based signals for filtration purpose. While considering its db family it has higher order high pass filters which gives information very efficiently about its coefficients. These filters are very useful

to extract information from transient signals. Wavelet transformation having time-frequency localization ability as compared with Fourier transform and it is best suited for non-stationary signals. Wavelet transform can be continuous or discrete depending upon the way the dilation and translation parameter are selected. Discrete wavelet transform (DWT) is more advantageous because it decomposes the signal into direct family of frequency band that do not overlap as in CW.

Generally faults occur in high frequency transient's signals, so that it necessary to detect and extract the high frequency component in current signals. Due to this we have to convert it into digital for wavelet transformation filtering operation. In this paper we developed fault classification system to detect and classify the fault by the use of wavelet transformation filtering to extract information and adaptive threshold techniques to detect nearest value of fault which was belonging to that type.

Generally fault occurs in high voltage transmission line which is above 25 KV. There are so many numbers of faults like distance protection operated, carrier fail, VT supply fail, auto reclose operated etc. Most occurring faults are belonging to distance protection operated fault. Such faults are phase related and ground related. There is 95% occurrence of ground related faults these faults include single line to ground, double line to ground, and line to line fault.

2. Wavelet Transform

The alternating current signals from transmission line system are non-stationary and random signals so it is very difficult to extract hidden information from it. Wavelet transform which is new tool for caballing both time and frequency information simultaneously.

The mother wavelet $\psi(t)$ is given as [6]:

$$\Psi(i,j)(t) = 2^{-j/2} \psi(2^{-j}t - k) \quad (1)$$

The coefficient of WT $C(m, t)$ are define by the following Inner product [7]

$$C(m, t) = 1/\sqrt{m} \int s(t) W_{t,t,m}(t) dt. \quad (2)$$

Where 'm' is scale factor and 's' is translation factor. Generally, WT consists of successive pairs of low- and high-pass filters. For each pair, the high-scale and low frequency components are called approximations, while the low-scale and high-frequency components are called details.

3. Logic for Fault Classification

In this paper we sampled out the current input signal with high sampling rate for various faults. The purpose of the k Nearest Neighbors (KNN) algorithm is to use a database in which the data points are separated into several separate classes to predict the classification of a new sample point. We sampled 10,000 values from fault associated input current signal. Depending upon its threshold value as compared with test signals by standard deviation mathematical formulae we can detect and classify which type of fault will occur. The difference of actual value and the test signal will give us the nearest threshold value. The proposed logic uses wavelet transform for extracting the hidden information in the current wave forms when a fault occurs, which is then suitably transformed to extract fault signatures and characterize the faults.

3.1 Analog Signal Processing

The input current signal from power system is analogous in nature so it is necessary to convert into digital form in order to do further processing. Hence signal processing is the first stage of proposed system. For 50 Hz system the frequency which is more suitable is 0 to 1000 Hz. The 2KHz sampling frequency is used to extract signals from this band. The processing unit is design such that it extracts band of frequencies and converted to digital form. The main component of signal processing are-1) Transducers and isolation 2) anti aliasing filters to avoid interferences 3) sampled and hold 4) multiplexers and 5) A to D conversion

3.2 Wavelet Decomposition

To extract high frequency transients information the three phase current signals are fed through wavelet decomposition filter. Here only single level of decomposition was employed rather than multilevel decomposition. For the detection and classification of faults the choice of mother wavelet is very important consideration. Daubechies (db) wavelets are the wavelets which are most commonly used for protection applications. For this paper db6 wavelet is used which is basically a high pass filter so the output of filter gives high frequency details.

3.3 Fault detection

The power system is in general subjected to a lot of disturbances So the first step is to detect these disturbances. A disturbance is detected in a phase current signal if the absolute value of the first difference of the high frequency detail coefficients is greater than threshold value. This logic for phase A is represented by the following

$$D_A(n) = 1, |HF_A(n) - HF_A(n-1)| > Th_d(1)$$

0, otherwise

Here HF- high frequency coefficient of phase A The Detect signal goes high, if a disturbance is detected in any one of the three-phase currents. For this system we keep threshold fix i.e 18 mV, phase related faults having its fixed threshold value depend upon its sampling frequency, A to D conversion rate & wavelet used. But ground related faults doesn't having its fixed threshold value it will change accordingly, hence we used peak magnitude detector for adaptive threshold technology.

3.4 Fault Classification

In this paper KNN method used for a classification purpose. In KNN, the learning step is trivial: we simply store the dataset in the system's memory. In the classification step, we are given an instance q (the query), whose attributes we will refer to as q. A_i (Attribute) and we wish to know its class. The harmonic spectra are obtained through application of DWT on one cycle of the measured voltage signals after fault beginning. The fault Classification related to each new pattern can be estimated through the KNN algorithm based on existing patterns. In KNN, the class of q is found as follows:

1. Find the k instances in the dataset that are closest to q.
2. These k instances then vote to determine the class of q.

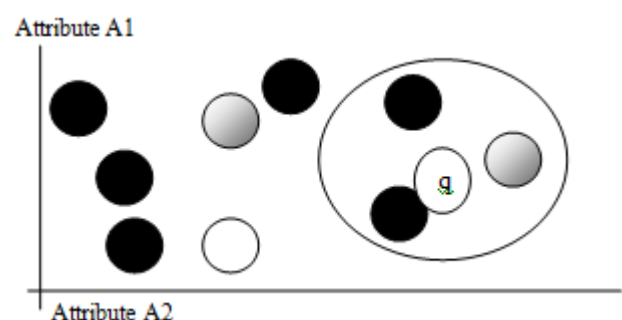


Figure 1: KNN classifier general case

Ties (whether they arise when finding the closest instances to q or when voting for the class of q) are broken arbitrarily. In the following visualization of this method, we assume there are only two attributes A1 and A2, and two different classes (where circles with solid fill represent instances in the dataset of one class and circles with hashed fill represent instances in the dataset of the other class). Query q is here being classified by its 3 nearest neighbours

3.4.1 KNN algorithm

As discussed earlier, we consider each of the characteristics in our training set as a different dimension in some space, and take the value an observation has for this characteristic to be its coordinate in that dimension, so getting a set of points in space. we can consider the similarity of two points to be the distance between them in this space under some appropriate metric. The way in which the algorithm decides which of the points from the training set are similar enough to be considered when choosing the class to predict for a new observation is to pick the k closest data points to the new observation, and to take the most common class among these. This is why it is called the K-Nearest Neighbours algorithm. The algorithm can be summarized as;

- 1) A positive integer k is specified, along with a new sample
- 2) We select k entries in our database which are closest to our new sample
- 3) We find the most common classification of these entries
- 4) This is the classification we give to the new sample

The general procedure for classifier is presented in Figure 2. The Classification algorithm applied to the high frequency details (in terms of normalized values). To reduce the hardware requirement, a simple Classification technique is used.

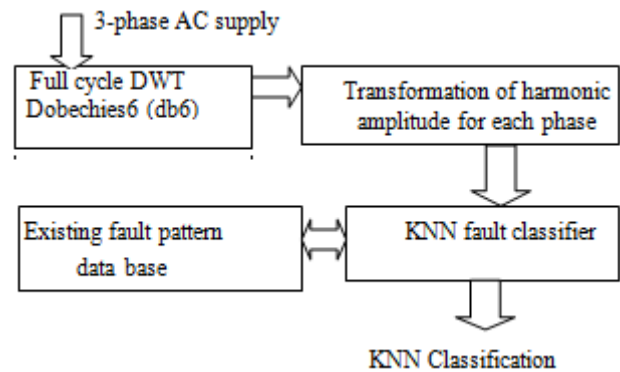


Figure 2: KNN classifier

4. Block diagram of Proposed Scheme

In this paper we used the concepts of transient fault extraction by Wavelet and suitable classification method with adaptive threshold technology and K- nearest neighboring algorithm. The following figure 3 shows block diagram for proposed scheme. Any intentional or unintentional change in an electrical net-work is accompanied by transients, which is a natural process by which the power system moves from one steady state condition to another. The duration of transients can vary from a few microseconds to milliseconds and can be broadly classified into those having an impulsive or an oscillatory nature. A fault typically causes a low frequency oscillatory type of transient, the spectral content of which is less than 5 kHz [1], before settling into the post fault steady state condition. The typical duration of this transient, which has a wealth of information embedded in it, is 0.3 to 50 ms and has a range of zero to four per unit [1]. The system design logic uses wavelet transform for extracting the hidden information in the current waveforms when a fault occurs, and KNN for fault Classification

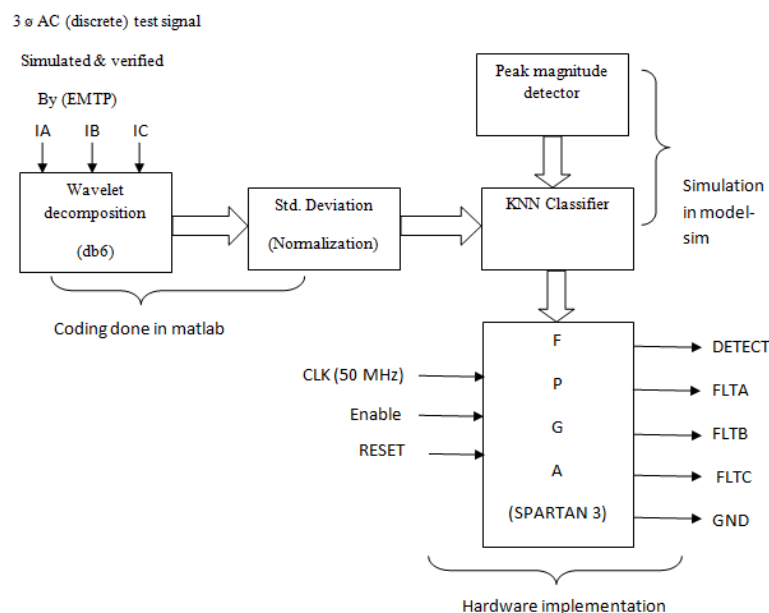


Figure 3: Block diagram for proposed scheme

5. Hardware Implementation

The hardware implementation of the proposed algorithm was done using FPGA. FPGA consists of a matrix of logic

elements which can be interconnected by the user to implement a given application in any desired fashion. As FPGAs can be reconfigured dynamically, it is possible to use them for more complex task achieved by other processors.

FPGA come in wide variety of sizes with advanced features. FPGA is mainly composed of three types of elements; configurable logic blocks (CLBs), input/output blocks (IOBs), and programmable interconnects (PIs). User implement logic function for given application through CLBs, by interfacing external package pins to the internal logic using IOBs and routing the paths for connecting CLBs and IOBs into network with the PIs.

5.1 FPGA design flow

FPGA design flow mainly consists of design entry, synthesis, and implementation and FPGA device programming. At the design entry stage, the behavior of the FPGA device is described by means of a hardware description language (HDL) like Very high speed integrated circuit HDL or Verilog. The design is synthesized to get an intermediate file called a net list. The net list is translated and mapped, which fits the design into the available resources on the target device. The place and route tool then places and routes the design according to the timing constraints. Programming file generation tool creates a bit stream file, referred as bitmap that can be downloaded to the device. Design verification which includes both functional and timing verifications, can be done at different points during the design flow. The main advantage of FPGA is ability to construct highly parallel structures for processing data. Also its performance is not associated to the clock rate but to the amount of parallelism that can be brought in the algorithms like DSP. FPGA allows design to be modified even after deployment in an end application. FPGA provides flexibility in defining arithmetic precision throughout computation and in implementing signal processing function. Finally, the software support for FPGA is also important consideration for that Xilinx: ISE WEBPACK series is used which provides full fledged support to FPGA design environment.

6. Experimental and Simulation Results

The proposed logic was first developed in the MATLAB environment. The wavelet decomposition filters were simulated with the filter blocks available in DSP block set. The power system was modeled in Electromagnetic Transients Program/Alternative Transients Program (EMTP/ATP). Various types of faults, like line to ground LG (AG, BG, CG), double line to ground LLG (ABG, BCG, ACG), line to line LL (AB, BC, AC), and three-phase faults LLL (ABC), were created, and the test waveforms for the proposed method were obtained. These sample values were imported to MATLAB environment. The Wavelet decomposition filter reduces 10000 input samples to 5000 as db6 wavelet is used as mother wavelet. After passing it through the normalization we are able to analyze its transient related information. After detecting the high frequency components by wavelet these signals were sent through KNN classification for proper classification of faults amongst all.

6.1 Test System

The logic was tested by using a system modeled in EMTP and simulating various fault conditions in ModelSim. Fig.5 shows waveform for fault line to ground at phase 1 (LG1) and Fig.4 shows waveform for fault LLG1 and Table.1 shows the sampled values at different samples for LG1 & LLG1, & ideal case condition i.e. expected values. If we calculate its voltage difference by formula;

V_{temp1} = voltage at 8500 in LG1

V_{temp2} = voltage at 8500 in normal condition

So, Voltage Difference = Voltage at LG1 - Voltage at normal

Voltage Difference = 0.088579 - 0.014195
= 0.074384

Under the knowledge of above result for voltage difference, we have shown the following table.2 where we get the approximated voltage value i.e. 0.074384 which is minimum difference and used as threshold value for detection of fault, then KNN algorithm is applied as compared to this value to the LG1 fault samples selected. After matched this value to the LG1 fault samples gives us the fault type of that particular instances. For LLG1 and remaining faults same formula can be applied. In case we get the negative value suppose ($V < 0$) then simply add this negative value to the normal value, we will get the same result as LG1. In this logic there are two types of threshold adaptive and fixed. For a three phase fault there is no changing in its threshold, & its occurrence in transmission line is only about 5%. The next part is the Graphical user interfaced (GUI) for this system. In fig.5. we have shown the waveform from wavelet toolbox of original LG1 fault signal, its synthesized signal along with single level decomposition. The reason behind the modelsim is concern, it read the discrete data files from matlab and perform operation on it. Fig6. Shows simulation results from modelsim when fault LG1 is detected.

Finally the experimental results regarding device utilization summary of FPGA device. Xilinx: ISE WebPACK-8.1i was used to synthesize and implement the design into the FPGA chip. The general purpose SPARTAN 3 FPGA kit, which has an XC3S500E-4- FG320 IC developed by Xilinx Inc. was used for prototype development because of its cost effectiveness. The XC3S500E4FG320 chip has over 10000 logic cells and 232 user I/O pins. It has onboard Universal Serial Bus- based FPGA download/debug interface and 50-MHz clock oscillator. The entire power system modeling is done using EMTP/ATP, and the waveforms are available as data files in the computer. The standard parallel port was used for applying the digital signals from a computer to the FPGA kit.

Table I: Voltage levels at different samples values

Sr. No.	Sample points	LG1(A)	LLG1(B)	Normal(Z)
1.	8500	0.088579	0.088649	0.014195
2.	8501	0.087619	0.087677	0.014359
3.	8502	0.086636	0.085668	0.014519
4.	8503	0.085632	0.084632	0.014675

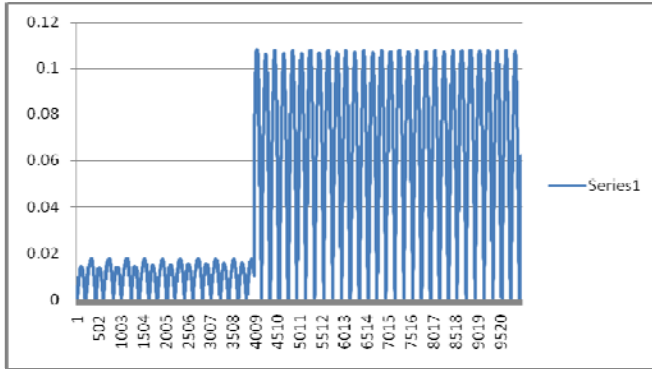


Figure 4: waveform for fault LLG1

Table II: Result for voltage difference for LG1

Sr. No.	Sample Points	Detected voltages
1.	8513	0.074472
2.	8713	0.074857
3.	8811	0.074629
4.	8913	0.074472
5.	9113	0.074859
6.	9211	0.074628

The inputs to the FPGA chip for the present application are *Clock*, *Reset*, *Enable*, and three-phase input current signals. The main output signals are the *Detect* and 11 different types

of faults. The FPGA device utilization details given in table 3 which shows Logic Utilization and table 4. which shows logic distribution. It can be observed that only 30% of the slices of a moderate sized device are utilized for this application. The total number of IOBs used is 7. Fig 7. shows Top level RTL Schematic. The synthesis report shows specifications as source done (FF), destination: done(PAD), source clock: CLK rising, total gate delay as 54.764 ns for (34.204ns logic, 20.560ns route), total memory usage as 2,36,912 kilo bytes. The system gives 100% accurate results for *LG*, *LL*, and *LLL* (i.e., *ABC*) types of faults. In the case of *LLG* faults, there were some misclassifications. But it can be seen that the probability of occurrence of *LLG* faults is only 5%. Hence, it can be safely expected that the system will give an overall accuracy of 99.53%.

Table III: Logic Utilization

Sr. No	Logic utilization	Used	Available	Utilization
1	No. of sliced flip/flop	384	4896	7%
2	Number of a i/p LUT	666	4896	13%

Table IV: .Logic Distribution

Sr. No	Logic distribution	Used	Available	Utilization
1.	4 I/P Lookup tables	1441	4896	29%
2.	Occupied Slices	745	2448	30%
3.	Bonded Iob	7	158	7%

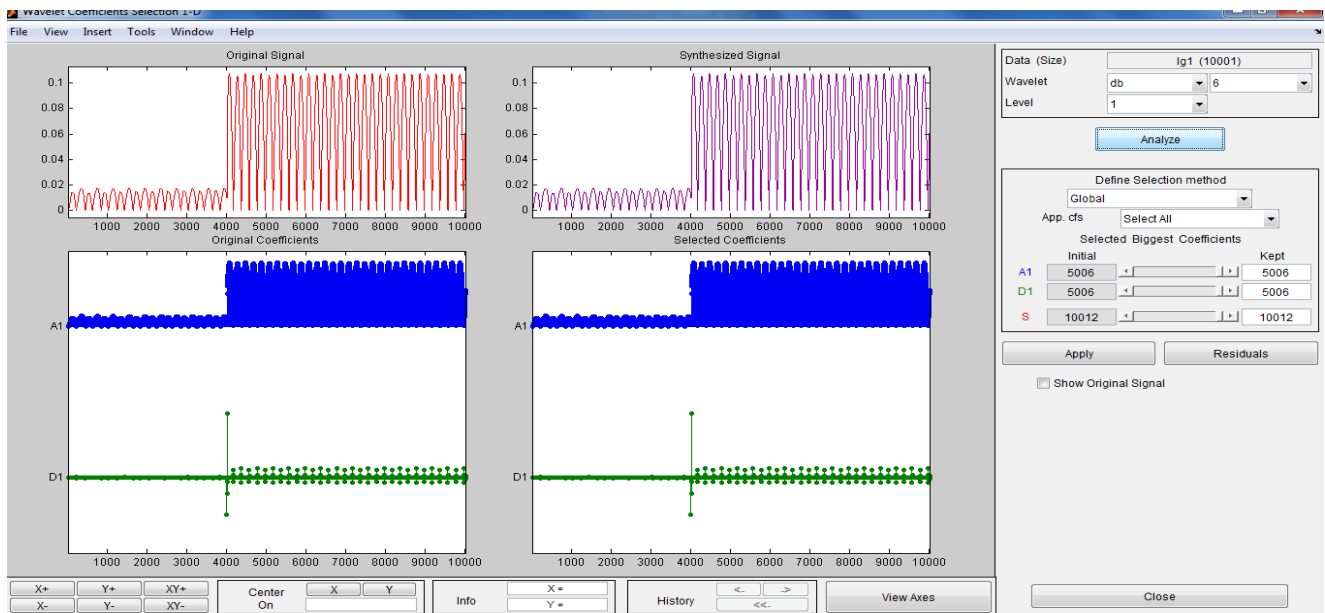


Figure 5: Waveform from wavelet toolbox

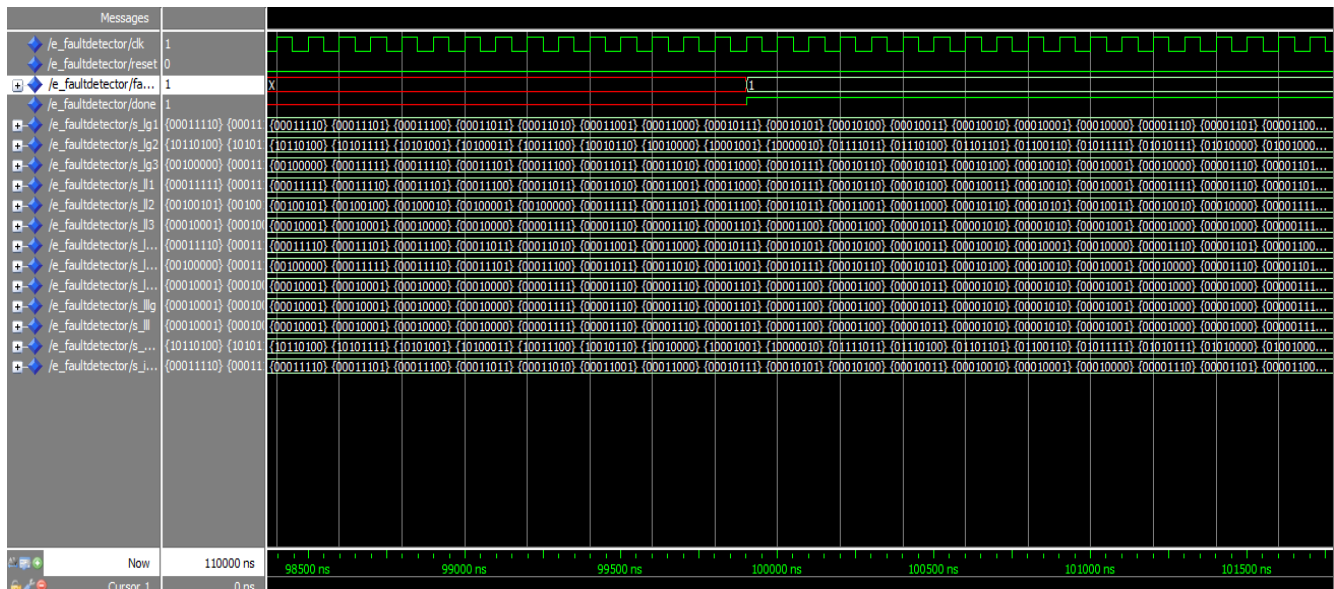


Figure 6: Simulation results from modelsim when fault LG1 detected



Figure 7: Top level RTL Schematic

7. Conclusions

A novel technique for fault detection and classification from transmission line is proposed. The logic is first developed in MATLAB environment to wavelet transform which extracts high frequency details from signals and processes the high frequency details to give information about the faults. The important features of proposed technique are as follow 1) Only a single db6 wavelet filter is used for each phase 2) Adaptive Threshold and KNN algorithm is used 3) Adaptive calculation of threshold is involved which is used for classification purpose 4) No complicated energy calculations are involved 5) Modelsim is used for simulation purpose 6) The logic is easy to implement on SPARTAN3 FPGA board. FPGA provide an affordable customized option for testing the performance of new protection technique. FPGA are reusable if in case design problem detected at testing stage the chip can be reprogrammed after certain change were made in the design It has been verified through various EMTP/ATP simulated fault cases that the system operation is fast, highly reliable, and secure.

References

- [1] C. J. Kim and B. D. Russell, "Classification of faults and switching events by inductive reasoning and expert

- system methodology," *IEEE Trans. Power Del.*, vol. 4, no. 3, pp. 1631–1637, Jul. 1989
- [2] B. Das and J. V. Reddy, "Fuzzy-logic-based fault classification scheme for digital distance protection," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 609–616, Apr. 2005
- [3] H. Wang and W. Keerthipala, "Fuzzy-neuro approach to fault classification for transmission line protection," *IEEE Trans. Power Del.*, vol. 13, no. 4, pp. 1093–1102, Oct. 1998.
- [4] M. M. Mansour and G. W. Swift, "A multi microprocessor based travelling wave relay—Theory and realization," *IEEE Trans. Power Del.*, vol. PWRD-1, no. 1, pp. 272–279, Jan. 1986.
- [5] W. A. Wilkinson and M. D. Cox, "Discrete wavelet analysis of power system transients," *IEEE Trans. Power Syst.*, vol. 11, no. 4, pp. 2038–2044, Oct. 1996
- [6] W. Chen, O. P. Malik, X. Yin, and Z. Zhang, "Study of wavelet-based ultra high speed directional transmission line protection," *IEEE Trans. Pow. PoweDel*
- [7] Simi P. Valsan and K. Shanti Swarup, High-speed fault classification in power lines: Theory and FPGA based Implementation, *IEEE Trans. on industrial electronics*, VOL. 56, No., 5, MAY. 2009
- [8] C. Fan, K. K. Li, W. L. Chan, and W. Yu, "Study of protection scheme for transmission line based on wavelet transient energy," *Int. J. Elect. Power Energy Syst.*, vol. 28, no. 7, pp. 459–470, Sep. 2006
- [9] P. M. Silveria, R. Seara, and H. H. Zurn, "An approach using wavelet transform for fault type identification in digital relaying," in *Proc. IEEE Power Eng. Soc. Summer Meeting*, 1999, pp. 937–942.
- [10] Y. Liao and S. Elangovan, "Fault noise based approach to phase selection using wavelets based feature extraction," *Elect. Power Compon. Syst.*, vol. 27, no. 4, pp. 389–398, Apr. 1999.
- [11] O. A. S. Youssef, "Combined fuzzy-logic wavelet-based fault classification technique for power system relaying," *IEEE Trans. Power Del.*, vol. 19, no. 2, pp. 582–589, Apr. 2004.

[12] Xilinx Data Sheets. [Online]. Available:
<http://direct.xilinx.com/bvdocs>

Author Profile



Sumit S Chincholkar has completed B.E. (Electronics and telecommunication) from Amravati university, Maharashtra, India in 2011. Presently he is pursuing M.E. (Electronics) from MGMs Jawaharlal Nehru Engineering College, Aurangabad (M.S.), India.



Dr. Syed A. Naveed is Professor in the Department of Electronics, Jawaharlal Nehru Engineering College, Aurangabad (M.S.), India. He has completed B.E. (Electrical, Electronics & Power), M.E. (Electrical Power System) and Ph.D. (Electrical & Electronics Engineering) in 2000, 2001 and 2009 respectively. He has more than 12 years of experience in technical field at various levels in academics. He has 29 national/ international technical publications. He is Fellow Chartered Educator from University Euro American Consortium, Madrid, Spain, 2013. He is Chartered Engineer with IE, Chartered Valuer with IIV and Chartered Industrial Environmentalist with SES. He has been presented "Rajiv Gandhi Excellence Award" on 24-08-2013 at New Delhi and conferred with "The Best Citizens of India Award" in 2013