International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2014): 5.611

Simulation of High-Efficiency AC/DC Converter with Quasi-Active Power Factor Correction

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Abstract: ***Power Factor is an important performance parameter of a system and improving power factor is very much essential for the better and economic performance of the system. This paper presents a novel ac/dc converter based on a quasi-active power factor correction (PFC) scheme. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc flyback converter. Operating principles, analysis, and simulation results of the proposed method are presented.***

Keywords: AC/DC converter, power factor correction, single stage.

1. Introduction

Conventional offline power converters with diode– capacitor rectifier have resulted in distorted input current waveforms with high harmonic contents. To solve these problems, so as to comply with the harmonic standards such as IEC 61000-3-2, several techniques have been proposed to shape the input current waveform of the power converter. A common approach to improving the power factor is a two-stage power conversion approach.The two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed. These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation.

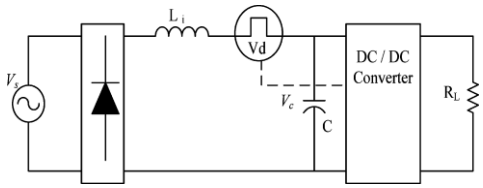

Figure 1: General Circuit diagram of dither rectifier with PFC cell

Usually, the DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields slightly higher efficiency compared to the DCM operation. A detailed review of the single-stage PFC converters is presented. Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation. In addition, although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and high as well as wide-range intermediate dc bus voltage stress to overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented in which a high frequency ac voltage source (dither signal) is connected in series with the rectifier input voltage in order to shape the input current (see Fig. 1).

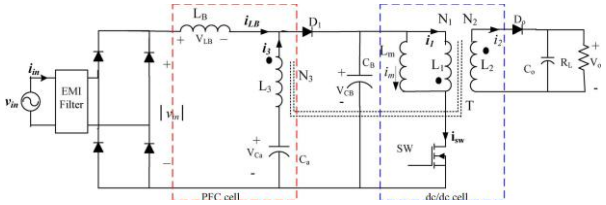

Figure 2: Proposed quasi-active PFC circuit diagram.

Another technique based on parallel connection of this dither signal is presented; however, the harmonic content can meet the regulatory standard by a small margin. A new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values. In this letter, a new technique of quasi-active PFC is proposed. As shown in Fig. 2, the PFC cell is formed by connecting the energy buffer (LB) and an auxiliary winding (L3) coupled to Fig. 2. Proposed quasi-active PFC circuit diagram the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. The input inductor LB operates in DCM such that a lower THD of the input current can be achieved. The structure, operation principles, and analysis of the proposed converter are presented in Section II. Design example and the experimental results are presented in Section III.

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2. Proposed Quasi-Active PFC Circuit

The proposed quasi-active PFC circuit is analyzed in this section. As shown in Fig. 2, the circuit comprised of a bridge rectifier, a boost inductor LB, a bulk capacitor Ca in series with the auxiliary windings L_3, an intermediate dc-bus voltage capacitor C_B, and a discontinuous input current power load, such as flyback converter. The flyback transformer (T) has three windings N_1, N_2, and N_3. The secondary winding N_2 =1is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high-frequency pulsating source. The quasi- active PFC cell can be considered one power stage but without an active switch. To simplify the analysis, the following assumptions have been made:

1) All semiconductors components are ideal. According to this assumption, the primary switch and the rectifier do not have parasitic capacitances and represent ideal short and open circuits in their ON and OFF states, respectively.
2) The power transformer does not have the leakage inductances because of the ideal coupling.
3) All the capacitors are high enough so that the voltage across them is considered constant.
4) Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line frequency.

A. Principles of Operation of the Proposed Circuit

To facilitate the analysis of operation, Fig. 3(a) and (b) shows the topological stages and the key waveforms of the proposed circuit. It is assumed that both the input inductor LB and the magnetizing inductance of the flyback converter operate in DCM. Therefore, currents i_{LB}, i_m, and i2 are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage V_{Ca} is greater than the average rectified input voltage $|v_{in}|$. To ensure proper operation of the converter, the transformer's turns ratio should be $(N_3/N_1) \geq 2$ and the boost inductor $L_B < L_m$. In steady-state operation, the topology can be divided into four operating stages.

1) Stage 1 ($t_o - t_1$):
When the switch (SW) is turned on at to, diodes D_1 and D_o are OFF, therefore, the dc-bus voltage VCB is applied to the magnetizing inductor Lm, which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{Vcb}{Lm}(to - t1) \quad (1)$$

and since diode D1 is OFF, the input inductor LB is charged by input voltage, therefore, the inductor current iLB is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as

$$i_{LB} = \frac{|Vin| + \left(\frac{N_3}{N_1}\right)Vcb - Vca}{LB} = (to - t1) \quad (2)$$

where, Vin = Vm |sinθ| is the rectified input voltage, (to −t1)=dTS is the ON-time of the switch (SW), LB is the boost inductor and N1, N3 are the primary and auxiliary turns ratio, respectively. At this stage, iLB = −i3 and the capacitor Ca is in the charging mode. On the other hand, Do is reversed biased and there is no current flow through the secondary winding. Since the transformer is assumed ideal, based on Ampere's law, it has

$N_1 i_1 + N_2 i_2 - N_3 i_{LB} = 0$

Where i2 =0at this stage therefore,

$$i_1 = \left(\frac{N3}{N1}\right) i_{LB} = \left(-\frac{N3}{N1}\right) i_3 \quad (3)$$

$$\text{Thus, } i_m = i_{CB} - i_1 = i_{CB} + \left(\frac{N3}{N1}\right) i_3 \quad (4)$$

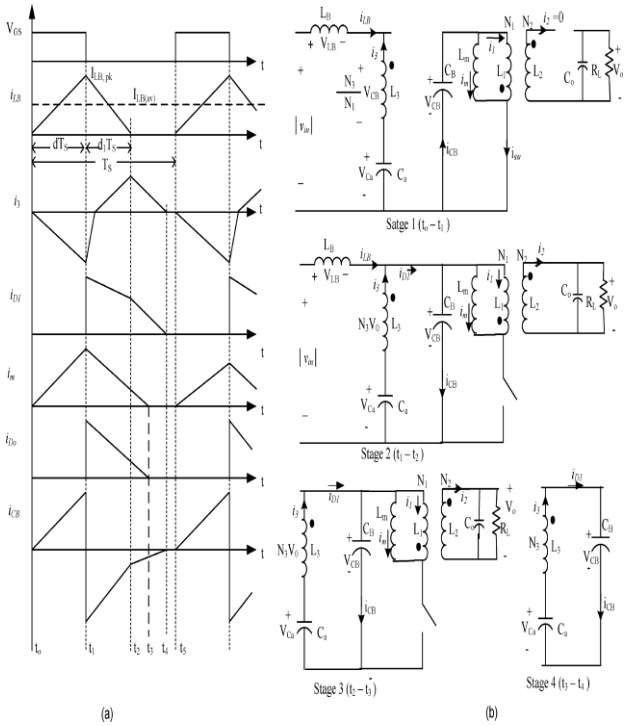

Figure 3: (a) Key switching waveforms of the proposed PFC. (b) Equivalent circuit operation stages of the proposed PFC circuit during one switching period.

Therefore, from (4) it can be seen that the magnetizing current im is supplied by the discharging current from the dc bus capacitor CB and the current i3 which is equal to input current iLB at this stage. The current through the main switch (SW) is given by

$$i_{sw} = i_{CB} = i_m - N_3/N_1\, i_3 = i_m + N_3/N1\, i_{LB} \quad (5)$$

Therefore, the current stress of the switch can be reduced by selecting the turn's ratio (N3/N1), which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter [11], the switch current is given by

$$i_{sw} = i_m + i_{LB} \quad (6)$$

Obviously, the proposed circuit has less switch current stress, therefore, the conduction loss and switching losses are reduced, and the efficiency is improved correspondingly. This stage ends when the switch is turned off at t = t1.

2) Stage 2 (t1 −t2):
When the switch is turned OFF at t =t1, output diode Do begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. Similarly, the diode D1 is also forward biased and the voltage across LB now Vin− VCB. Therefore, the current ILB is linearly decreased to zero at t = t2 (DCM operation), and the energy stored in LB is delivered to the dc bus capacitor CB. Therefore,

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$$i_{LB} = \frac{|Vin|+Vcb}{LB}(t_1-t_2) \quad (7)$$

The capacitor (Ca) is also discharging its energy to the dc bus capacitor CB and the current i3 reverse its direction. Therefore, the capacitor current is given by

$$i_{D1} = i_{CB} = i_{LB} + i_3 \quad (8)$$

3) Stage 3 (t2 −t3):
At this stage, the input inductor current iLB reaches zero and the capacitor Ca continues to discharge its energy to the dc bus capacitor CB. Therefore, iD1 = iCB =i3. At t = t3, the magnetizing inductor releases all its energy to the load and the currents im and i2 reach to zero level because a DCM operation is assumed.

4) Stage 4 (t3 −t4): This stage starts when the currents im and i2 reach to zero. Diode D1 still forward biased, therefore, the capacitor Ca still releasing its energy to the dc bus capacitor CB. This stage ends when the capacitor Ca is completely discharged and current i3 reaches zero. At t = t5, the switch is turned on again to repeat the switching cycle.

B. Steady-State Analysis

The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors and the input–output power balance as explained in the following. From the volt-second balance on LB

$$(V_{in}+\frac{N3}{N1}V_{CB} - V_{Ca})\,dTs = (V_{CB} - V_{in})\,d_1Ts \quad (9)$$

where d1 is the OFF-time of the switch (SW). Therefore, d1 could be given by

$$d_1 = \frac{Vin+\left(\frac{Ns}{N_1}\right)Vcb-Vca}{Vcb-Vin}\,d \quad (10)$$

From Fig. 3(a), the average current of the boost inductor in a switching cycle is given by

$$I_{in} = I_{LBav} = \frac{iLB,peak}{2}\,(d+d1)\,Ts \quad (11)$$

Substituting for iLB, peak given in (2) and using (10), the average input current is given by

$$I_{in} = \frac{Vin+\left(\frac{Ns}{N_1}\right)Vcb-Vca}{2LB}\,d2Ts \times \frac{(1+\left(\frac{Ns}{N_1}\right)Vcb-Vca}{Vcb-Vin} \quad (12)$$

Based on (12) for a given input voltage, Fig. 4(a) shows the normalized input current waveform in a half cycle for a change in the turns ratio (N3/N1). It can be seen that to reduce the dead time and improve the power factor of the input current the turn's ratio must be ≥0.5. Similarly, Fig. 4(b) shows the normalized input current waveform for a change in dc bus capacitor voltage VCB. As it can be seen that the higher the VCB the better quality of the input current waveform (lower THD). However, higher VCB means higher voltage stress on the power switch (SW), which can reduce the efficiency of the converter. Therefore, a trade off between THD and efficiency must be made. The energy absorbed by the circuit from the source during a half switching cycle is given by

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} Vm\,\sin(t)\,Iin\,dt \quad (13)$$

Substitution for Iin in given (12) yields

$$Pin = \frac{1}{\pi}\frac{Vm}{2LB}\,d2Ts(A)\int_0^{\pi}\sin(t)\,Bdt$$

Where

$A = [(1+N_3/N_1)\,V_{CB} - V_{Ca}]$,

$$B = \frac{Vm\,\sin(t)+\left(\frac{Ns}{N_1}\right)Vcb-Vca}{Vcb-Vm\,\sin(t)}$$

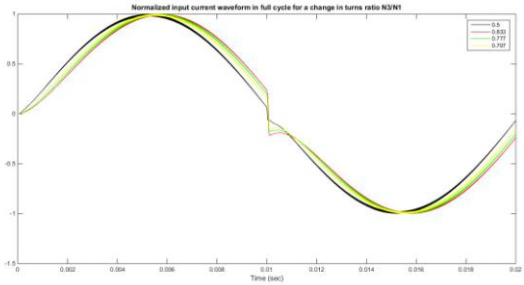

Figure 4: Normalized input current waveform in half cycle for a change in turns ratio N3/N1

The average output power for a DCM flyback converter is given by

$$P_0 = \frac{V2cb}{2Lm}\,d^2Ts \quad (14)$$

Assume 100% efficiency, Pin = Po, yields

$$V^2_{CB} = \frac{Vm}{\pi}\frac{Lm}{Lb}(A)\int_0^{\pi}\sin(t)B\,dt \quad (15)$$

Above equation (15) shows that the dc bus capacitor is independent of load variation; VCB is determined by the input voltage and circuit parameters Lm/LB, N3/N1. Note that the transcendental and can only be solved by numerical method using specific circuit parameters.

3. Simulation Results

Ratings of the active power factor corrector:

- Input voltage : 230 V AC
- Operating frequency : 50 Hz
- Load Resistance = 100 ohms
- Inductor value (L_{B1})= 1 µH
- Output capacitor = 4700 µF

3.1 Proposed MATLAB Circuit

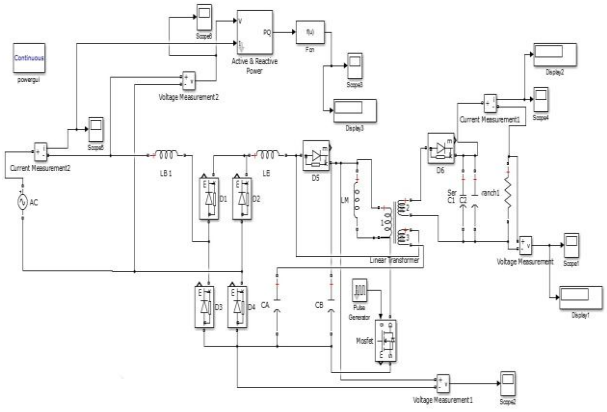

Figure 5: MATLAB Simulation model for ac-dc converter active power factor correction

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3.2 Simulation Results

a) Input Voltage:

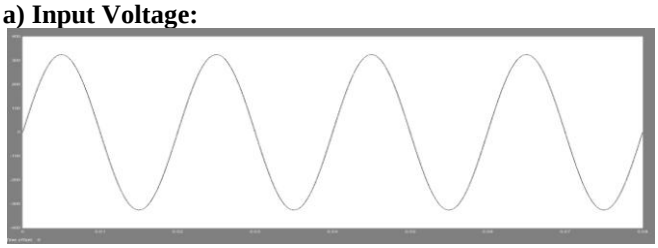

Figure 5.1: Input Voltage (volts)

b) Rectified Output Voltage with PFC:

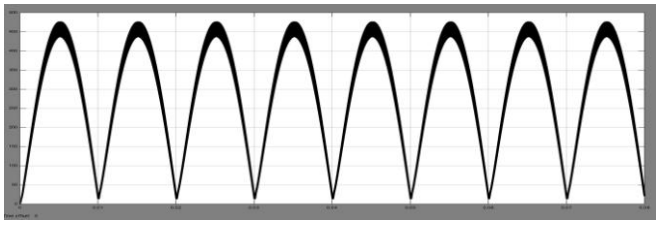

Figure 5.2: Rectified Output Voltage with PFC (volts)

d) Input Current Power Factor with PFC:

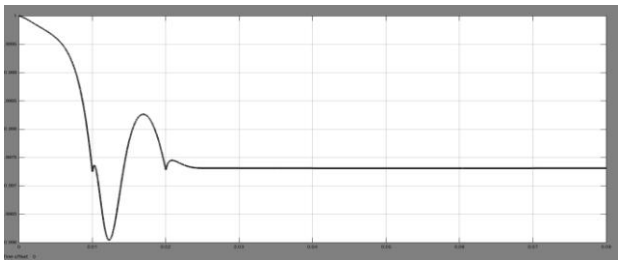

Figure 5.3: Input Current Power Factor with PFC (amperes)

e) Voltage across the load with PFC:

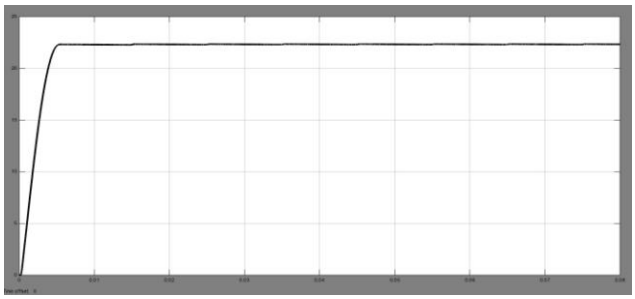

Figure 5.4: Load Voltage with PFC

f) Total Harmonic Distortion with PFC:

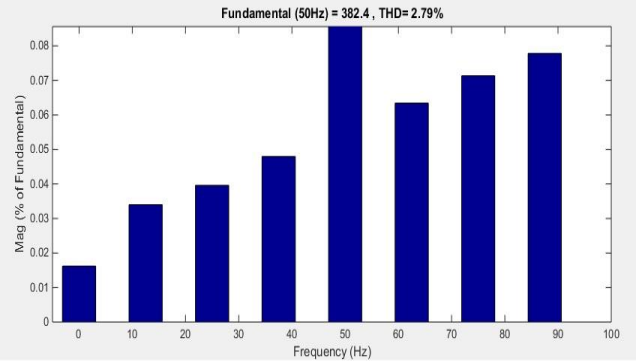

Figure 5.5: Input Current THD with PFC

Table 1: MATLAB Simulation Results with Resistive Load

Sr. No.	*Input Voltage*	*R Load*	*Power Factor*	*O/p Current*	*Output Voltage*	*THD %*
1	230	3.9	0.9974	5.46	21.31	2.77
2	230	4.7	0.9974	4.63	21.77	2.75
3	230	6.9	0.9973	3.52	24.3	2.74
4	230	10.8	0.9973	2.14	23.12	2.79
5	230	560	0.9973	0.04	24.2	2.79

Table 2: MATLAB Simulation Results with Inductive Load

Sr. No.	*Input Voltage*	*L Load*	*Power Factor*	*O/p Current*	*Output Voltage*	*THD %*
1	230	1	0.9973	1.856	23.31	2.79
2	230	3	0.9973	0.6254	23.92	2.77
3	230	6	0.9973	0.3137	24.08	2.77
4	230	12	0.9973	0.1572	24.17	2.79
5	230	24	0.9973	0.0786	24.22	2.79

4. Conclusion

In this letter, a new ac/dc converter based on a quasi-active PFC scheme has been presented. The proposed method produces a current with low harmonic content to meet the standard specifications as well as high efficiency. This circuit is based on adding an auxiliary winding to the transformer of a cascade dc/dc DCM flyback converter. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a trade off between efficiency and harmonic content can be established to obtain compliance with the regulation and efficiency as high as possible. Operating principles, analysis, and experimental results of the proposed method are presented.

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