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Design of Low Power, Area Efficient and High Stability Multiple Frequency Output Phase Locked Loop for Multiphase Clocking Circuits

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Abstract: ***A phase locked loop (PLL) is a key element of many communication and instrumentation domain. It is a key element in clock generation. The proposed paper presents the design of low power, area efficient and high stability multiple frequency output of PLL using high performance and low power VCO for fast frequency locking. The PLL is designed in Microwind EDA in design environment using 32nm CMOS technology with operating frequency of 1 GHz and lock time of 100ns. We are using high performance VCO with wide frequency range of 1.59 GHz to 3.52 GHz. The PLL consumes total power of 0.118 mw with the technology supply voltage of 1 V. The PLL is designed with multiple output frequency locking as 3.67 GHz, 1.87 GHz, 0.86 GHz, and 0.42 GHz with an efficient area as 57.5µm2.***

Keywords: Phase-locked loop, Phase frequency detector, low pass filter, voltage controlled oscillator, CMOSetc.

1. Introduction

The Phase locked loop is a feedback control system which maintains the phase and frequency of output signal and reference signal constant [1]. It is a basic building block used in communications system such as mobile phones, motor speed control, optical disk drive etc. The primary goal of the PLL is to produce a clock which has same phase and frequency as that of reference clock. Once the phase and frequency are matched PLL goes into locked state. This is accomplished by correcting error between the reference and feedback signal. The modern communication Engineering applications are designed to work on multiple frequencies, so the proposed PLL with four multiple output using CMOS 32 nm technology will be the best solution assuming low power and high stability. A PLL has blocks as shown in Figure 1.

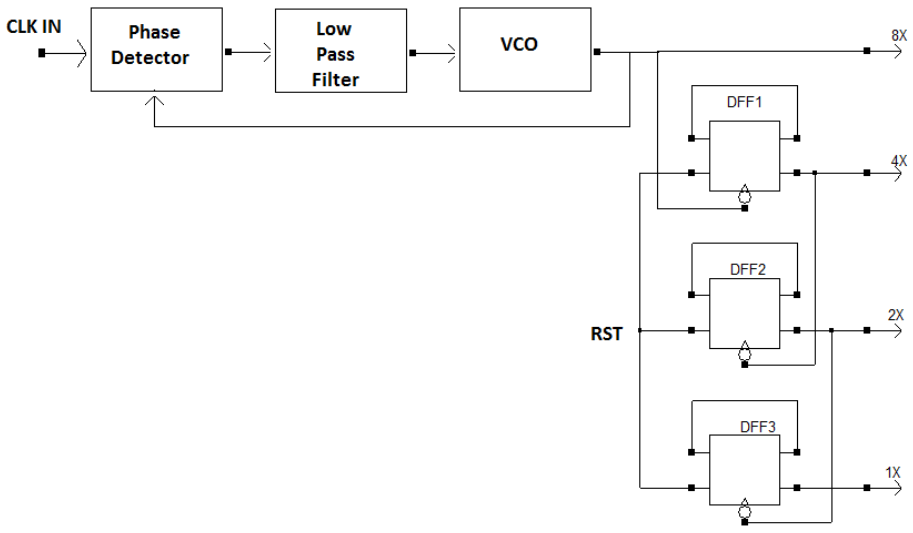

Figure 1: Block diagram of Multiple Frequency output PLL

The proposed PLL is a feedback system composed of three elements: a phase detector, a loop filter, a high performance voltage controlled oscillator (VCO) and network of D-Flip Flop providing multiple Frequency output. The design of Multiple Frequency Output Phase Locked Loop is a new concept and also found superior to all the conventional techniques. Since multiple output of PLL generates multiple clocks at a time, it can be useful for multi channelling wireless communication system or for multiphase clocking circuits. The proposed PLL will give four multiple outputs as PLL8x, PLL4x, PLL2x and PLL1x simultaneously, which in turn provides a very fast multitasking communication

The reference signal is periodic such as square wave which

is compare with the output of VCO using a phase detector. The output of phase detector is then applied to the low pass filter and used as a control signal to drive a VCO. The idea is that the VCO will lock onto reference signal thus can be used to tracked a periodic signal as its phase and frequency varies.

To obtain the proposed PLL design, CMOS circuit of each element of proposed PLL is converted into physical layout. After cascading the layout of each element, final layout is obtained. The proposed work is particularly focuses on analysis and design of phase-locked loop with low power consumption with multiple frequency output.

2. Design of Phase Detector

The phase detector compares the phase and frequency of the input and feedback signal [1]. As per the difference between these two signals, the phase detector is supplied with two inputs as clkDiv and ClkIn.

The phase detector of the PLL is the XOR gate [2] [4] [5]. The XOR gate output produces a regular square oscillation VPD when the clock input circuit and signal input divIn have one quarter of period shift (900 or π /2). For other angles, the output is no more regular. When the phase between clkDiv and ClkIn is around π/2, PDV is VDD/2, then it increases to VDD.

The XOR gate output produces a regulator square oscillation VPD when the clkin and the signal clkDiv have one quarter of period shift (90 or π /2). For other angles output is not regular [7].

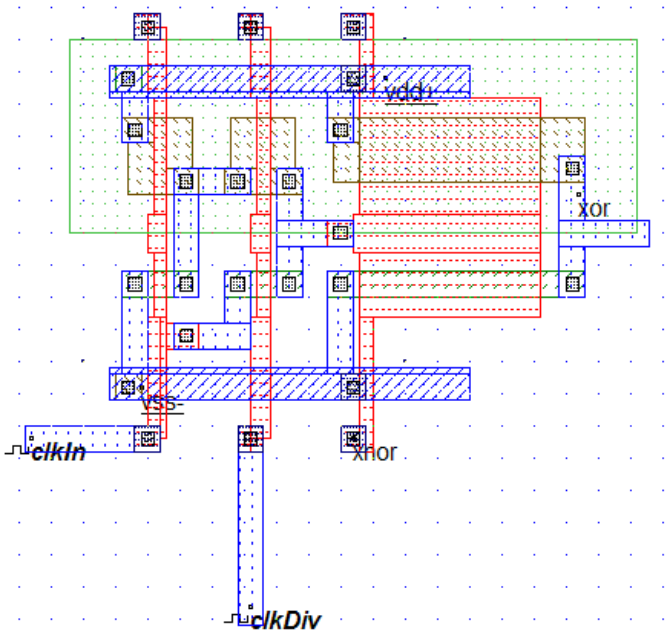

Figure 2: Physical design of Phase Detector

3. Low Pass Filter

The low pass filter is used to transform the instantaneous phase difference VPD into an analog voltage Vc which is equivalent to the average voltage VPD [3]. The rapid variations of the phase detector output are converted into a slow varying signal Vc which will later control the voltage controlled oscillator [3]. Without filtering, the VCO control would have too rapid changes which would lead to instability.

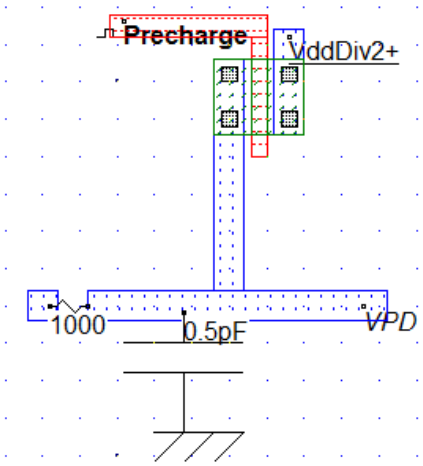

Figure 3: Physical design of Low pass Filter

The filter may simply be a large capacitor C, charged and discharged through the Ron resistance of the switch. The RonC delay creates a low-pass filter.

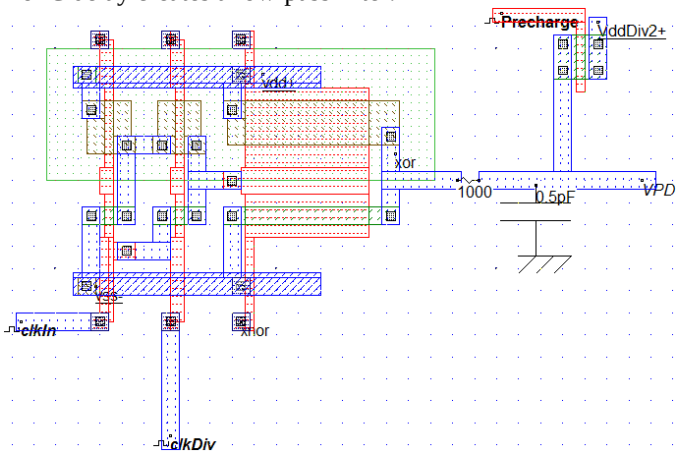

Figure 4: Physical design of Phase Detector with Low pass Filter

4. Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO is commonly used for clock generation in phase lock loop circuits. The VCO design is based on an inverter-type ring oscillator supplied by a current coming from the voltage-to-current converter [5]. The VCO consists of five-stage fully differential delay cells performing full switching. Phase noise [5], tuning range, power consumption and device size are the main areas to be considered while designing any VCO circuit. Nowadays, the VCO designs are made in such a way that greater emphasis is on reducing power consumption, so it is difficult to achieve low phase noise and wide tuning range because of more emphasis on the low-power VCO designs [12].

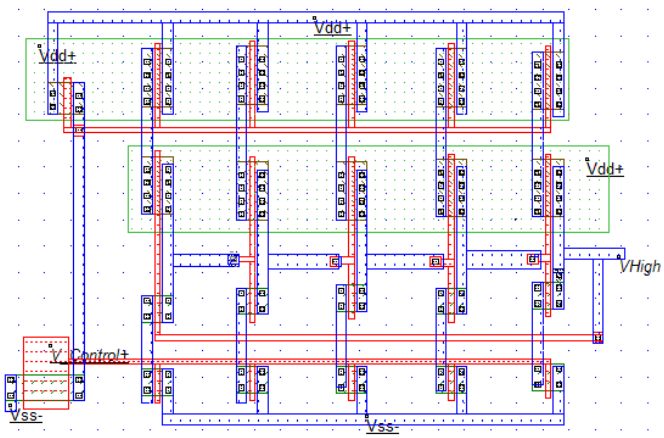

Figure 5: Physical design of proposed VCO

The current-started inverter chain uses a voltage control Vcontrol to modify the current that flows in the N1, P1 branch. The current through N1 is mirrored by N2, N3, N4, N5 and N6. The same current flows in P1. The current Through P1 is mirrored by P2, P3, P4, P5 and P6. Consequent by the change in Vcontrol induces a global change in the inverter currents and acts directly on the delay. Here, we have five inverters in the loop but it is possible to put more, it depends on the oscillating frequency required.

5. Phase Locked Loop

After cascading the layout of each sub-element, final PLL design layout is obtained.

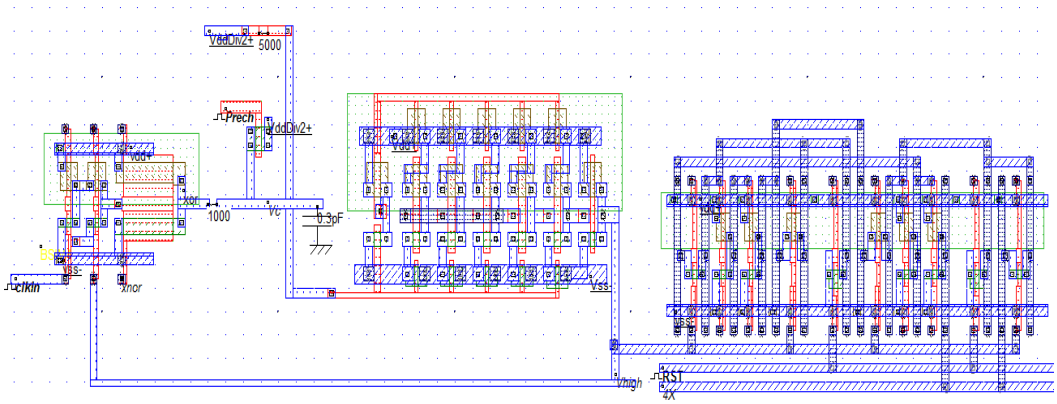

Figure 6: Physical design of proposed PLL

For multiple frequency output PLL, frequency of clkin is get divided by two at the output div2. For the output section of proposed PLL, the output of VCO Vhigh is represented by 8x. The other outputs 4x, is obtained by cascading the output of 8x as input to divided by 2 network D-flip flop. 2x is obtained by giving the output 4x as a input to another D-flip flop. And 1x is obtained by giving the output 2x as input to another D-flip flop.

6. Simulation Results

The Phase Detector output produces a regulator square oscillation VPD when the clk and the signal divin have one quarter of period shift. The simulation result of the phase detector is shown in figure 7 below.

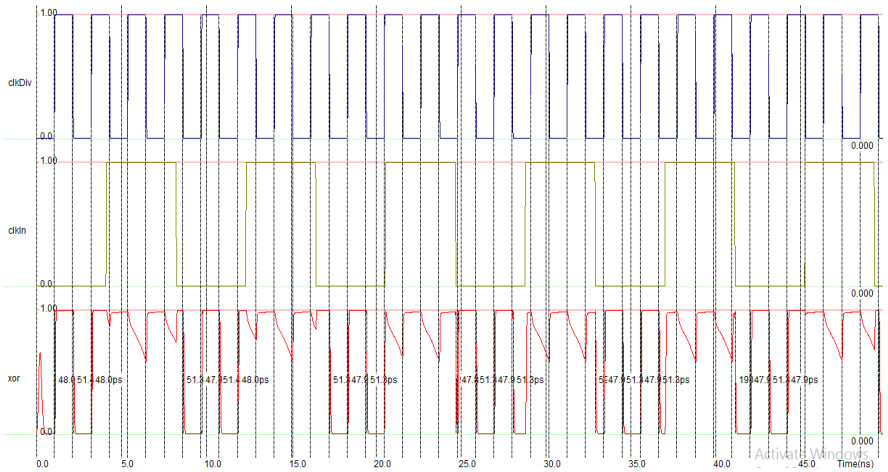

Figure 7: Simulation result of PD

The filter is used to transform the instantaneous phase difference VPD into an analog voltage Vc which is equivalent to the average voltage VPD as shown in figure 8.

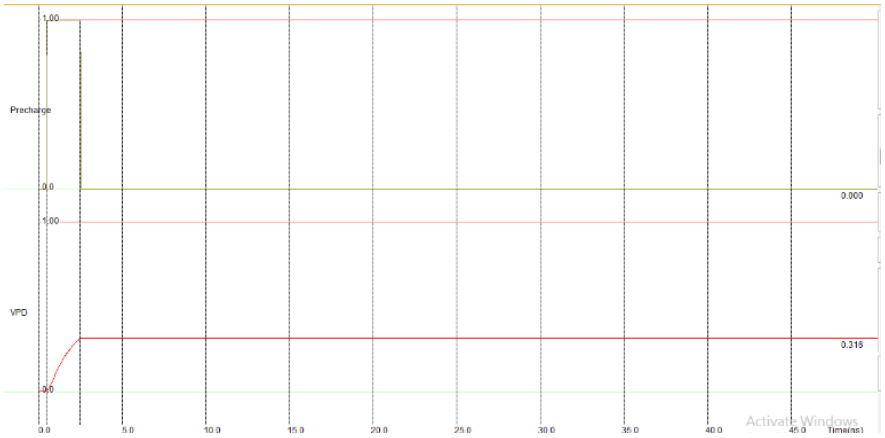

Figure 8: Simulation result of Filter

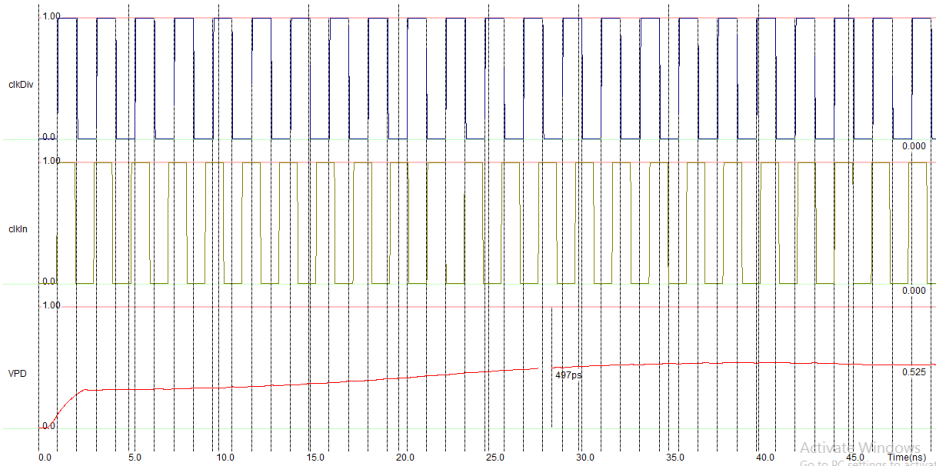

Figure 9: Simulation result of Phase Detector with Filter

The voltage variations of input signal 'V_control' and output signal 'Voltage_ctr_osc' are given in Fig.9. We chose to modify V_control very slowly, in order to see the influence on the oscillations. We put Control higher than 0.5 V, because there are no any oscillations under that value.

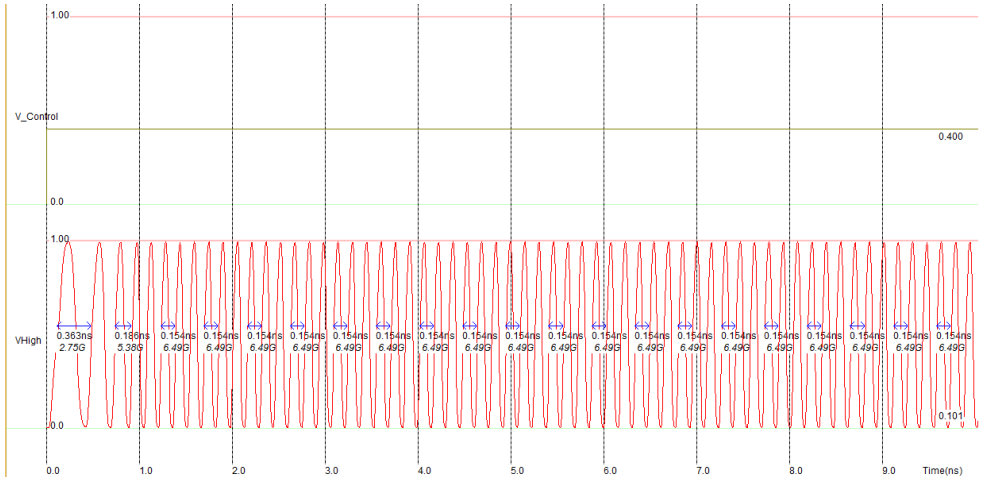

Figure 10: Simulation result of VCO

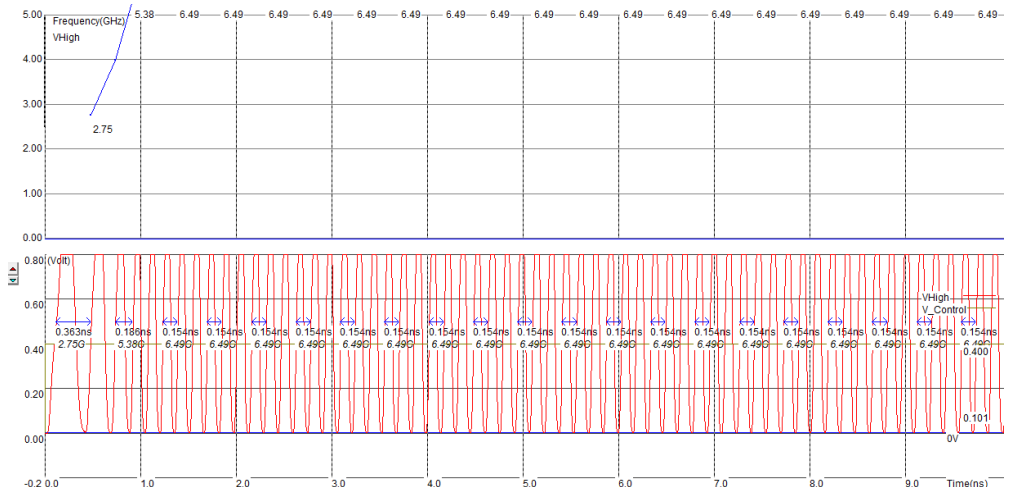

Figure 11: Simulation result of VCO

The designed VCO provides the stable frequency of 6.49GHz (figure 11) which is provided as the second input to the proposed PLL. Figure 12 shows the four frequency output as 1X, 2X, 3X and Vhigh (8X) for the proposed PLL design.

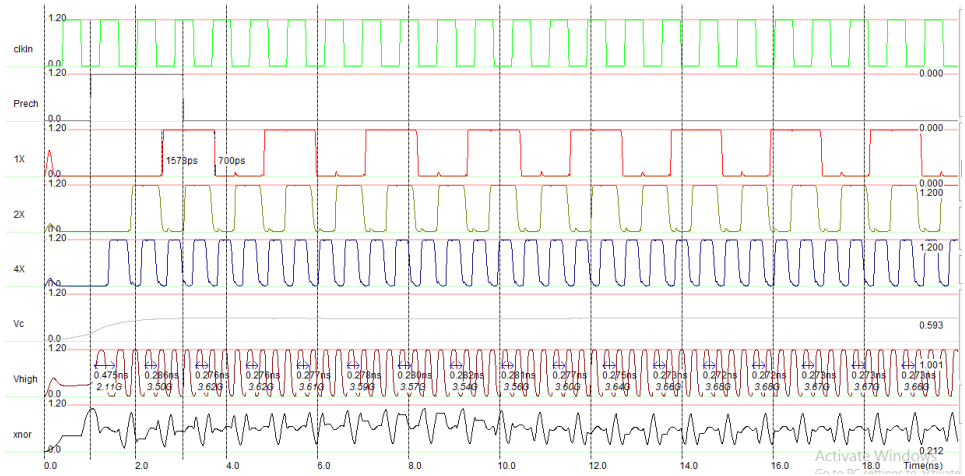

Figure 12: Simulation result of PLL

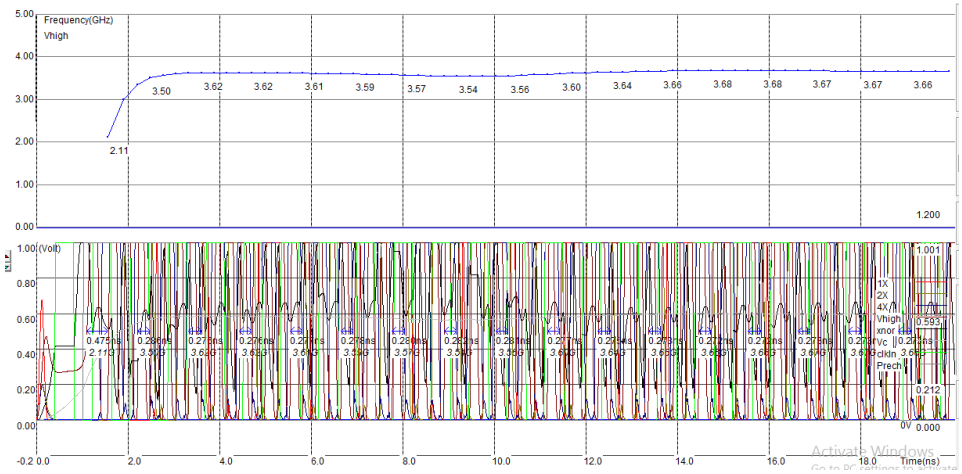

Figure 13: Frequency verses time of response of PLL

7. Result Analysis

For observing the stability of the proposed PLL, there is variation of supply VDD from 0.6V to 1V, the output of PLL remained stable. It proves the high stability of the PLL. From the parametric analysis of designed PLL the power dissipation measured by VDD at 1V is found to be 0.118mw, which shows that power consumption is also very low (Low power).

VDD (V)	8X (Freq. (GHz)	4X (Freq. (GHz)	2X (Freq. (GHz)	1X (Freq. (GHz)
0.6	3.67	1.87	0.86	0.42
0.7	3.67	1.87	0.86	0.42
0.8	3.67	1.87	0.86	0.42
0.9	3.67	1.87	0.86	0.42
1.0	3.67	1.87	0.86	0.42

8. Conclusion

The proposed work is aimed to design transistorized CMOS physical layout of Phase locked loop to achieve for Low power, area efficient, high stability Phase Locked Loop. The design of Multiple Frequency Output Phase Locked Loop is a new concept and also found superior to all the conventional techniques.

The proposed project is also plan to work on low supply voltage of 1volt. By observing the output of PLL at each node with the voltage variation of supply voltage from 0.6 volt to 1 volt. The expected output frequency of each node must be remained same. This results will prove the stability of the proposed PLL.

The proposed design is very high efficient, low power optimum area phase locked loop with four multiple outputs as PLL8x, PLL4x, and PLL2x & PLL1x of 3.67 GHz 1.87 GHz, 0.86 GHz, and 0.42 GHz respectively.

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