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Streamlining VLSI Physical Design Engineering with SART: An Automated Tool for Data Extraction and Report Generation

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Abstract: ***SART, an automation tool tailored for VLSI Physical Design Engineers, streamlines, and accelerates the data extraction and report generation process. It specifically targets the Specified flow, considering its directory structure. Instead of manual data extraction from reports and manual report creation, SART simplifies these tasks by automatically running the flow, generating reports, and collecting essential information for reports or Excel sheets. This tool is versatile, capable of handling various functions such as running the flow, generating reports, data extraction, and report creation in different formats based on user preferences. Additionally, it offers email notifications to relevant users. SART is implemented using multiple programming languages, including Python, Tcl, and Perl, which are commonly used in the VLSI physical design field. It also supports partitioned statistics and reports, facilitating multi-user operations and status tracking.***

Keywords: SART, VLSI - Physical Design, APR-flow, Sign-off-flows, Python, Perl, Tcl

1. Introduction

The major critical task for the physical design engineer occurs after the APR run is completed. The task involves analyzing the logs and reports for errors and valid some checks in Reports, as well as creating Excel sheets for review during meetings.

When the client's RTL changes, physical design engineers have to manually initiate runs, extract reports, and create Excel sheets.

Copying and pasting the same report at every stage is a time-consuming and critical task. For each block partition, the owner may spend approximately 2-3 hours collecting all APR (Reports & Logs) and SIGNOFF (Extraction, VCLP, FEV, LV, STA, CALIBER) reports.

When a Team Lead is responsible for 'N' blocks' information collection and manual Excel sheet creation, it significantly increases the time required. While scripters can write scripts to collect data, the challenge arises when project scenarios change, necessitating manual adjustments each time. This is where SART comes into play; it's designed for such scenarios.

SART offers numerous possibilities, allowing physical design engineers to automate apr and sign-off's flows, extract information from reports, and easily generate reports. The tool efficiently handles large amounts of data in seconds. SART is built with fully automatic programming to save management time, enabling quick reviews of 'N' block information in less than 10 seconds.

1) APR & SIGNOFF flows dashboard's

The VLSI (Very Large-Scale Integration) Physical Design APR (Automatic Place and Route) flow is a series of steps and processes used to automate the

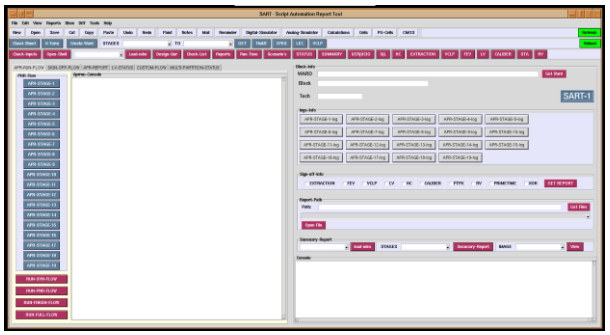

Figure 1: SART-(Script Automation Report Tool)

placement and routing of digital integrated circuits on a semiconductor substrate. This flow is critical for optimizing the physical layout of an IC design, ensuring it meets performance, power, and area constraints. Here's an overview of the VLSI Physical Design APR flow.

Design Netlist: The process begins with a design netlist, which is a representation of the digital circuit in terms of gates and their interconnections. This netlist is generated after logic synthesis.

Floor planning: In this step, the overall chip area is divided into functional blocks. Floor planning tools determine the approximate placement and dimensions of these blocks. Floor planning aims to optimize factors like wirelength, signal delay, and power consumption.

Placement: After floor planning, detailed placement tools are used to precisely place individual gates and flip-flops within each functional block. The goal is to minimize wirelength, ensure efficient use of space, and meet timing constraints.

Clock Tree Synthesis (CTS): A clock distribution network, known as the clock tree, is synthesized to ensure synchronous operation of the design. The CTS process optimizes clock buffer insertion and balances clock skew

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across the chip.

Global Routing: Global routing determines the high-level routing paths for critical signals. It identifies the general route that each net will take across the chip, including metal layer assignments.

Detail Routing: Detail routing, also known as global optimization or detailed routing, involves refining the routing of individual nets. It determines the precise routing tracks, vias, and layers for each net, considering congestion and design rules.

The apr run-flow window consists of a pnr-flow label category that includes all the apr stage flows. by clicking on each individual button, you can run the flow according to your requirements. it will work using the nbjob commands mode. alternatively, the user can run it in steps mode as follows:
run-syn flow: this switch helps run from starting ID to IP. (apr-stage-1 to apr-stage-6)
run-pnr-flow: this switch helps run from FP to RO. (apr-stage-7 to apr-stage-16)
run-finish-flow: this switch helps run from EF to finish. (apr-stage-17 to apr-stage-19)

There is one more option, **run-full-flow,** which runs the entire flow.

It functions as a flow tracer for the SART to execute the flow and provides the status of the running in the APR console window.

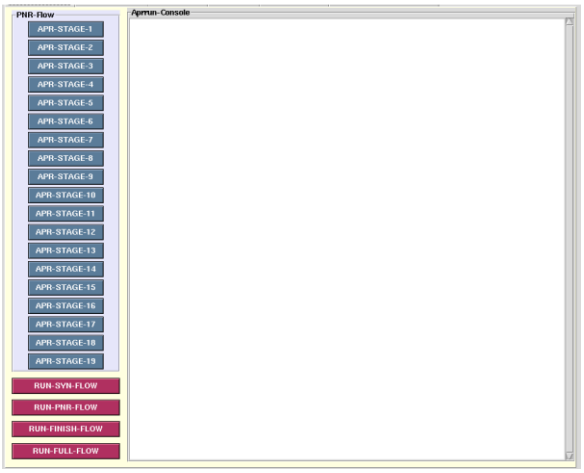

Figure 2: APR Flow- run Dashboard

EXTRACTION: Extraction is the process of extracting parasitic information from the layout of the design. Parasitic elements such as resistors, capacitors, and interconnect parasitic can affect the performance of the chip. Extraction tools generate models for these parasitic, which are then used for accurate timing analysis.

FEV (Formal Equivalence Verification): This is the initial stage of the physical design process where engineers verify that the RTL (Register-Transfer Level) design meets the functional requirements and specifications. It involves simulating and validating the logical functionality of the design before proceeding to physical design.

VCLP (Voltage, Clock, and Power Planning): This stage involves planning and optimizing the distribution of power, clock signals, and voltages throughout the chip to ensure proper operation and minimize power consumption.

Physical Verification: Physical verification encompasses various checks to ensure that the layout adheres to design rules, such as minimum feature size, spacing, and layer-specific rules. This stage helps identify and correct any layout errors that could lead to manufacturing defects.

Caliber: Caliber is a specific tool or suite of tools used for performing advanced physical verification and design rule checking. It helps ensure that the physical design is manufacturable and free from violations.

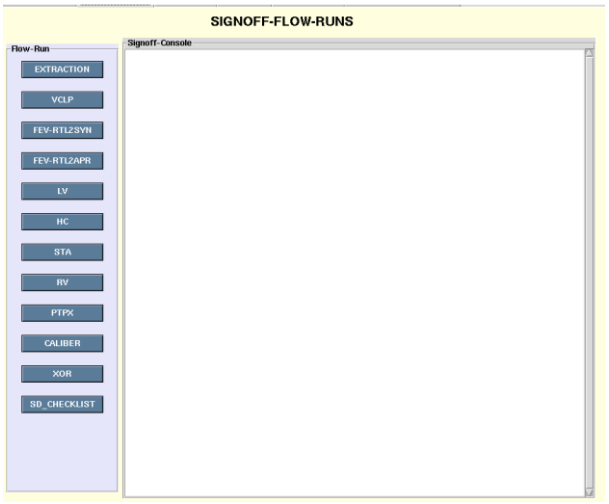

Figure 3: Signoff Flow- run Dashboard.

2) APR - Report Dashboard

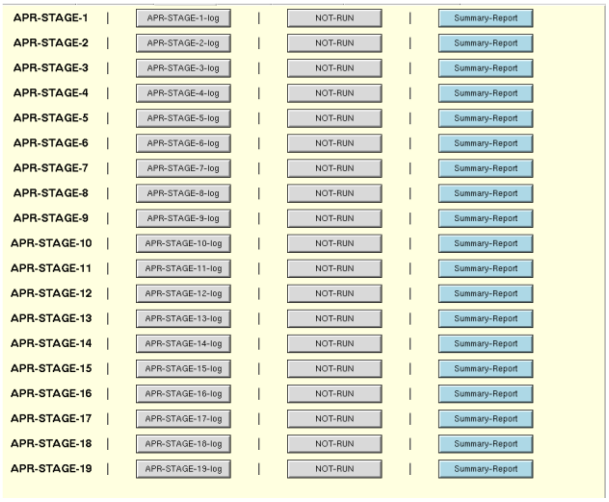

Figure 4: Block Partition APR - Report Dashboard.

Figure 4 above shows four columns of data:

1) The first column represents the labels of stages.
2) The second column represents the log information of the design. If a particular stage has errors in the log file, it is indicated with the color red. If there are no errors in the file, it is represented in green. If the file does not exist in that path, there will be no indication.

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3) The third column represents error information. Whatever errors are present in the log file will be displayed here, and users can easily identify them by the color indication and naming convention in that column. Users can also access the information by clicking the button.
4) The fourth column represents a summary of information for every stage. It gathers all the files from the required stage reports and compiles them into one sheet for quick reference by the user or management."

3) Multipartition Dashboard

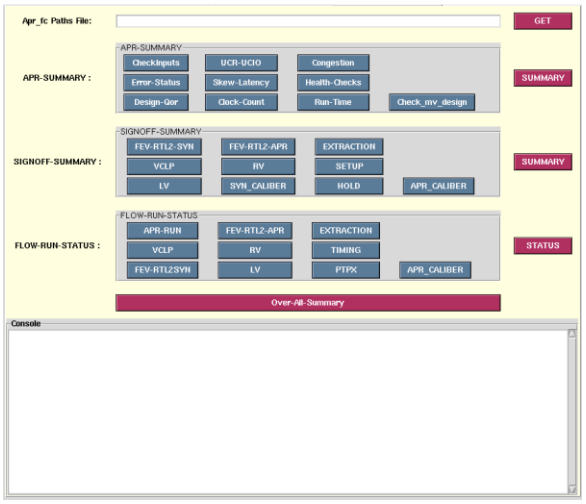


Figure 5: Multipartition - Report Dashboard

"Multipartition dashboard is designed especially for management purposes. A team lead or manager can easily review 'N' Blocks of information with a single click. It will generate reports in Excel, text, and GUI formats. By using this dashboard, a SART user can easily obtain information about all the blocks with color coding, making it simple to verify the validity of paths. Everything presented here below contains all the report information and what it collects from the dashboard of every switch."

Few switches were explained regarding their functionalities in the reports, including the information they collect.

Design_qor: This check collects important information from various stages of design quality of results (QoR) for all blocks and compiles it into an Excel sheet for quick verification.

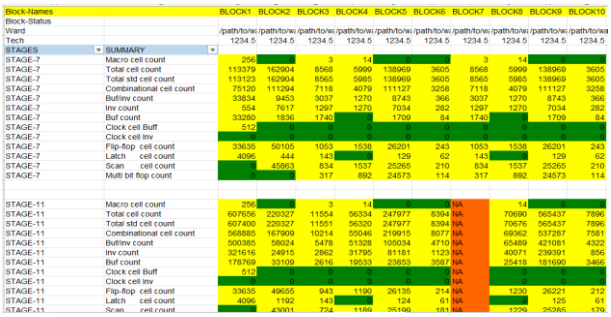
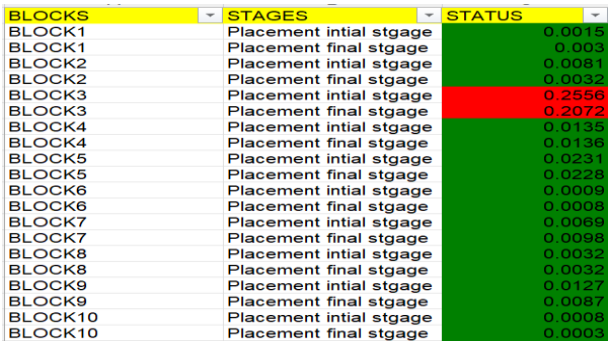


Figure 6: Multipatition Design-Qor Report

Congestion: This feature offers comprehensive congestion details for all blocks, indicating which blocks have higher congestion levels and which are congestion-less



BLOCKS	STAGES	STATUS
BLOCK1	Placement intial stgage	0.0015
BLOCK1	Placement final stgage	0.003
BLOCK2	Placement intial stgage	0.0081
BLOCK2	Placement final stgage	0.0032
BLOCK3	Placement intial stgage	0.2556
BLOCK3	Placement final stgage	0.2072
BLOCK4	Placement intial stgage	0.0135
BLOCK4	Placement final stgage	0.0136
BLOCK5	Placement intial stgage	0.0231
BLOCK5	Placement final stgage	0.0228
BLOCK6	Placement intial stgage	0.0009
BLOCK6	Placement final stgage	0.0008
BLOCK7	Placement intial stgage	0.0069
BLOCK7	Placement final stgage	0.0098
BLOCK8	Placement intial stgage	0.0032
BLOCK8	Placement final stgage	0.0032
BLOCK9	Placement intial stgage	0.0127
BLOCK9	Placement final stgage	0.0087
BLOCK10	Placement intial stgage	0.0008
BLOCK10	Placement final stgage	0.0003

Figure 7: Multipatition Congestion Report.

Flow-Run-Status:
Flow run status gives you overall summary of all the blocks what flows were run or not.

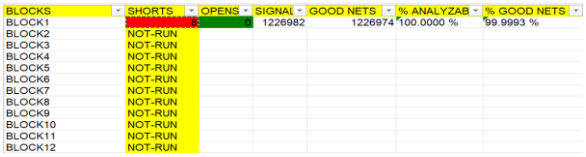
BLOCKS	FLOOR	PLACE	CTS	ROI	FINISH	EXTRACTIOI	FEVIRTL2S	VCLP	LV	CALIBER	STA
BLOCK1	YES	YES	YES	YES	YES	YES	YES	YES	YES	NO	NO
BLOCK2	YES	YES	YES	YES	NO	NO	NO	NO	NO	YES	NO
BLOCK3	YES	YES	YES	NO	NO	NO	YES	YES	NO	YES	NO
BLOCK4	YES	YES	YES	NO	NO	NO	YES	NO	NO	YES	NO
BLOCK5	YES	YES	YES	YES	YES	YES	YES	NO	YES	YES	NO
BLOCK6	YES	YES	YES	YES	YES	YES	YES	NO	NO	YES	NO
BLOCK7	YES	YES	YES	YES	YES	YES	YES	NO	NO	YES	NO
BLOCK8	YES	YES	NO	NO	NO	NO	YES	NO	NO	YES	NO
BLOCK9	YES	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO
BLOCK10	YES	YES	YES	NO	NO	NO	NO	NO	NO	NO	NO
BLOCK11	YES	YES	YES	YES	NO	NO	NO	YES	NO	NO	NO
BLOCK12	YES	YES	YES	YES	NO	YES	NO	YES	NO	NO	NO

Figure 8: Multipatition Flow-Run-Status Report

Caliber:

Figure 9: Multipatition Caliber Report

Extraction:



BLOCKS	SHORTS	OPENS	SIGNAL	GOOD NETS	% ANALYZAB	% GOOD NETS
BLOCK1	[redacted]	0	1226982	1226974	100.0000 %	99.9993 %
BLOCK2	NOT-RUN					
BLOCK3	NOT-RUN					
BLOCK4	NOT-RUN					
BLOCK5	NOT-RUN					
BLOCK6	NOT-RUN					
BLOCK7	NOT-RUN					
BLOCK8	NOT-RUN					
BLOCK9	NOT-RUN					
BLOCK10	NOT-RUN					
BLOCK11	NOT-RUN					
BLOCK12	NOT-RUN					

Figure 10: Multipatition Extraction Report

There are some additional checks (FEV, VCLP, LV, RV, TIMING) that include confidential rule names and clock names. These details are highly confidential, and SART will collect all the necessary data for multiple partitions as per the user's requirements.

4) Peo - Block - Info Dashboard

In this dashboard, engineers, Team Leads, and Managers can Review/access other data without needing to request reports' statuses from them. This information can be directly accessed from here by providing the WARD path, Block name, and Tech node.

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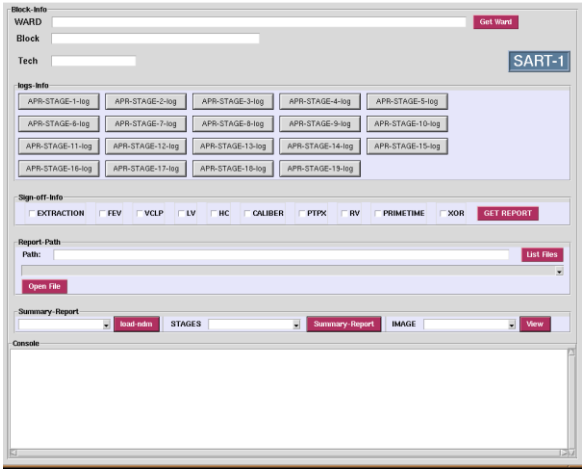

Figure 11: PEO – Block – Info Dashboard

Logs Information: Under this category, SART users can view logs information by entering the WARD path, block name, and tech node in the entry field above. The buttons will be color-coded as follows:

- Red indicates files with errors.
- Green indicates files without errors.
- Yellow indicates files that are not present in the specified directory. Engineers, Team Leads, or Managers can open their log files directly by clicking the respective buttons.

Report Path: In this category, users can easily review/access all files from any user's path right here. By entering the path in the 'Path:' field and clicking the 'List Files' button, all files in that directory will be displayed in the list box below. If an incorrect path is entered, it will be indicated as 'Invalid path' in the list box. Users can open a file by selecting it in the list box and clicking the 'Open File' button, making it easy to read the file.

Sign-off Info: In this category, we can view the summary of sign-off reports for any user, based on the specified ward path, block name, and tech node. By selecting the checkbox corresponding to the sign-off check used for review with SART, it will provide a summary report in text format containing both input and output information.

Summary Report: In this category, SART users can load there .ndm files by selecting the desired stage and clicking the 'Load NDM' button. The first list box will provide all stages from start to end, depending on the flow. The second list box offers all stages, allowing SART users to view the summary report of others' PEO by selecting the stage (pnr, apr, finish) and clicking the 'Summary Report' button, as shown in the figure. The final list box provides images of congestion maps, cell density, and pin density for specific stages, which users can view by selecting a stage and clicking the 'View' button.

5) SART Application's & Conclusion

a) Automated Flow Execution: SART handles the execution of the VLSI design flow seamlessly. No more manual intervention required.
b) Effortless Report Generation: SART takes care of generating reports without human involvement. This feature saves time and ensures accuracy.
c) Data Extraction Wizard: SART effortlessly extracts essential data from various sources, reducing the need for manual data extraction.
d) Report Customization: SART provides flexibility by allowing users to create reports in different formats according to their preferences. Whether it's Doc's, Excel sheets, or other formats, SART can generate reports to meet your specific needs.
e) Email Notifications: Keep your team in the loop with SART's built-in email notifications. Relevant users are alerted automatically, ensuring effective communication and status updates.
f) Multi-Language Support: SART is implemented using several programming languages commonly used in the VLSI physical design field, including Python, Tcl, and Perl. This versatility ensures seamless integration with existing workflows.
g) Partitioned Statistics and Reports: SART facilitates multi-user operations and provides partitioned statistics and reports. This feature aids in managing collaborative projects and tracking the status of different tasks within the flow.

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