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Reduction of Leakage Power for VLSI Design Logic Gate Circuits

Kiran Renukuntla

Department of Electronics and Communication Engineering, Jyothishmathi Institute of Technology and Science, Telangana State, India
rkiran5516[at]gmail.com

Abstract: ***High power dissipation has become key role in VLSI design circuits, when it comes to battery - operated applications it is important to save the battery life. Short - circuit power and switching power play key role in power dissipations, there are so many techniques to reduce power. By stacking arrangement, we can reduce power and we can utilize technique for various circuits. In this paper NAND and NOR gates realized, stacking technique consumes low power than standard reduction techniques. These circuits are simulated in Tanner EDA Tool with generic 250 nm transistors.***

Keywords: NAND gate, NOR gate, Leakage Power, STACK, CMOS Transistor

1. Introduction

In digital systems have increasing demands in the area of low power dissipation. area, power consumption, and delay are significant challenge parameters. High power consumption leads to reduce the battery life and requires more cooling and also costs packaging density. We can reduce the power by reducing activity factor, reducing capacitance, reducing voltage and decreasing frequency, reducing sizes of the devices and by using low load capacitance. In this paper low power ON transistor is used to reduce leakage power consumption.

$$P = \alpha * f * C * Vdd^2$$

Short circuit power is present short circuit path between supply voltage and ground and that is present difference in rise time fall times of input transition. Leakage power is present in MOS devices in static mode and dynamic mode. In static mode, leakage power present when circuit is not switching due to short channel and gate oxide thickness, we can decrease the leakage power by increasing threshold voltage but it decreases the device performance due to due to delay is introduced in the circuit. In dynamic mode also leakage power is present when circuit is in active mode and contributes more leakage power compared to active power whenever process technology is decreasing. Leakage power is significant when the channel length is reduced. So, we have to reduce power, we can reduce power by SAPON technique in which SAPON transistors remain in active.

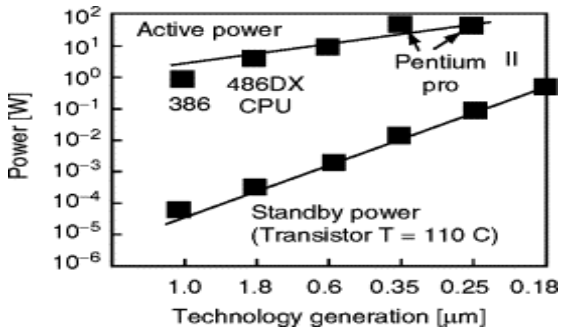


Figure 1: Power Vs Channel Length

2. Source of Power Consumption

Due to short circuit path current flowing from the power supply to the ground during switching, short circuit path power is present, we can reduce short circuit path by using variable threshold MOS transistors, To reduce leakage power in CMOS transistor we have more techniques such as stacking, power gating, MTCMOS and VTCMOS techniques are used. SC path consumes 15% power, switching power consumes 40 - 50% and Leakage power consumes 40 - 45%, so leakage power is important to reduce power dissipation. Large load capacitance is load to increase the speed of response at the output but due to this power dissipation occurs. By reducing the supply voltage threshold voltage is increased, due to this high threshold voltage leakage power is decreased.

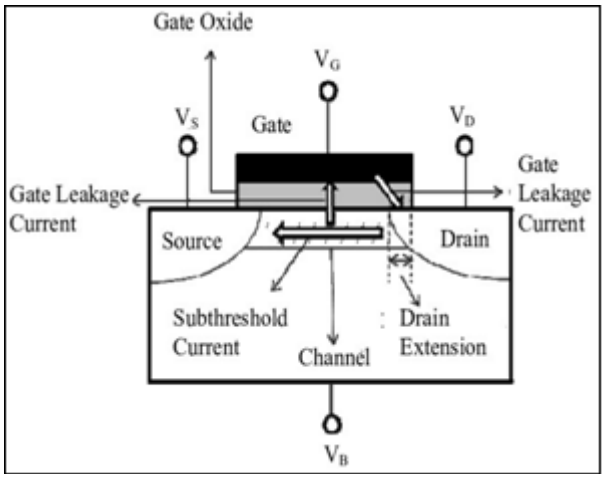


Figure 2: Leakage Currents

In CMOS transistor, both static and dynamic power are present, in static power leakage power is dominant power and in the case dynamic both switching and leakage power are important. There are so many techniques to reduce both static and dynamic power.

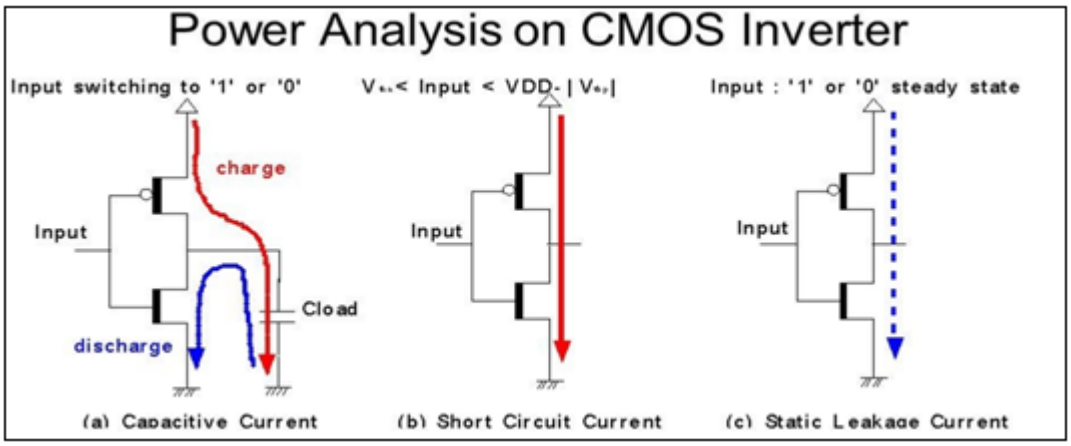


Figure 3: Short - Circuit Path Current

3. Proposed Technique

In this concise presents**,** leakage power reduction technique, in which extra PMOS and NMOS transistors are used. Transistor PMOS gate terminal is connected to the ground and NMOS gate terminal to the Vdd, which because they remain in the active region. EDA trainer tool is used to analyze power. In this two leakage control transistors (Q3&Q4) are built outside the circuit which increase the resistance between the Vdd and ground and also sub threshold leakage current is also reduced greatly.

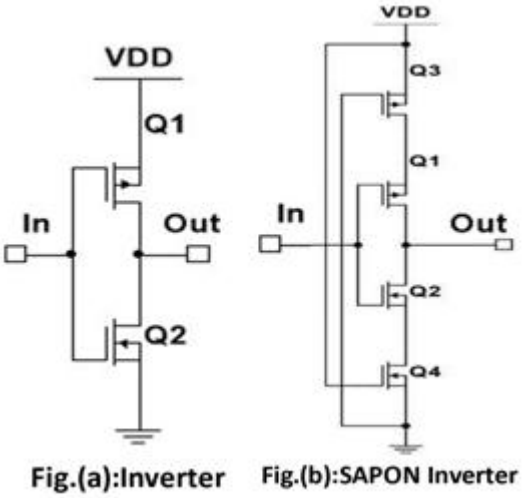
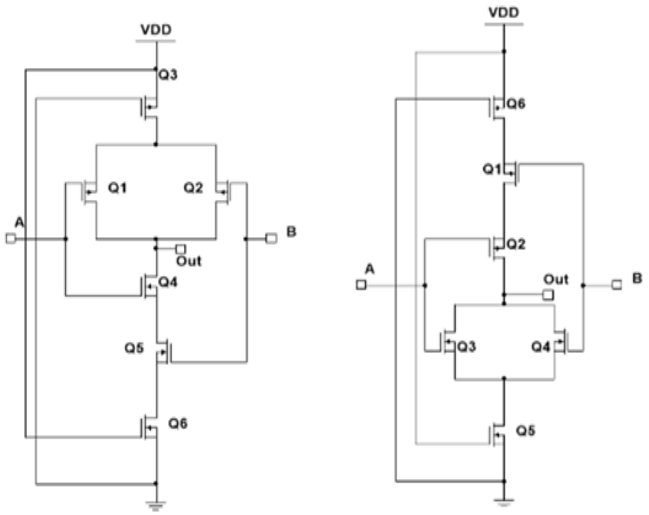


Figure 4: Leakage Power Reduction Technique

With THIS CMOS extra transistors power switching performance increased. SAPON PMOS is built above pull - up network and SAPON NMOS transistor is placed below pull - down network. These two extra transistors need to operate in an active region which in turn makes them active in all phases. Hence, it provides desirable output by maintaining low power consumption across circuits. When logic 0 is given PMOS transistor is on and NMOS transistor is OFF and SAPON transistors remain in active, output reads 1. Similarly, when logic 1 is applied PMOS is OFF and NMOS transistor is ON and SAPON transistors remain active output will be logic 0.



NAND and NOR gates:
Figure 5: NAND gate NOR gate

4. Simulation Results

Proposed technique reduces the leakage power 28% compared without extra transistors. It increases the speed of performance as both extra transistors are in active region proposed technique. NAND, NOR gate transient analysis is for given combination of inputs and simulation results are observed in Tanner EDA Tool.

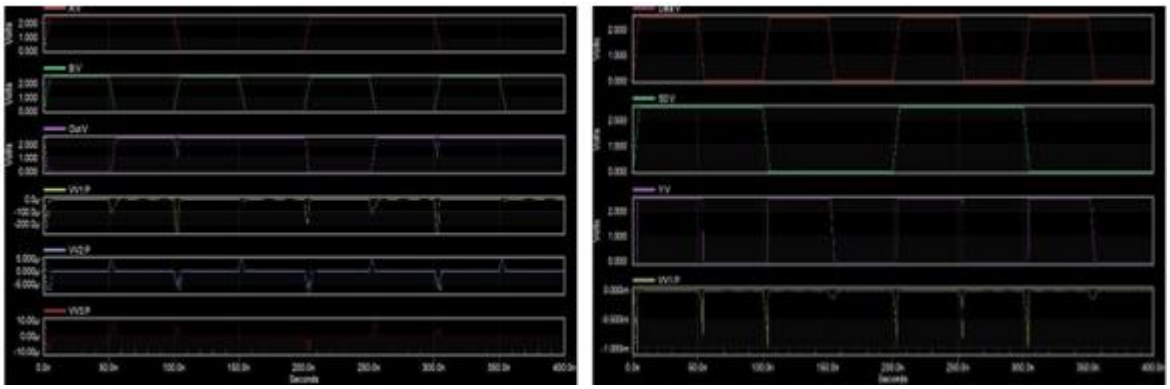


Figure (a): NAND gate **Figure (b):** NOR gate

Figure 6: Simulation Results

5. Conclusion

In low power VLSI circuits, power consumption plays key role to get optimize results. Using extra transistors (PMOS & NMOS) 28% power can be saved. It increases the speed if performance, saves energy and yields transition results better. We can reduce the power dissipation and can get better performance as channel length is decreased. It holds good for 10nm technology.

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Author Profile

Kiran Renukuntla received B - Tech degree from Vaagdevi College of Engineering, Warangal, completed M - Tech from Anasuya Devi Institute of Technology, Hyderabad. He has teaching field experience of nine years. Areas of interest include Embedded Systems, IOT and VLSI.