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Analyzing Performances of Ring Oscillator and Current Starved VCO in 90nm Technology

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Abstract: ***The performance of Ring Oscillator (CMOS RO) and Current Starved Voltage Controlled Oscillator (CS - VCO) in 90nm CMOS technology is thoroughly analyzed in this paper. The study involves a detailed examination of transient responses, parametric characteristics, and key performance metrics, such as delay, frequency, and power consumption. Our primary focus is on identifying optimal configurations for enhanced efficiency, with particular emphasis on understanding the impact of Inverter Stages on RO performance. Throughout systematic simulation and analysis, we aim to reduce power consumption while optimizing various parameters. Practical layouts for ROs and CS - VCOs are also designed to facilitate real - world implementation. The findings from this research contribute to the advancement of oscillator design in semiconductor technology, offering valuable insights for future circuit optimization endeavors. Power efficiency is paramount across all electronic systems, but it becomes especially critical in RF applications powered by batteries. These systems demand meticulous attention to detail to minimize power dissipation and extend operational life. In conclusion, we underscore the importance of power reduction as a key objective, and our analysis and conclusions will be based on its impact on overall efficiency and performance.***

Keywords: Ring Oscillator, 90nm CMOS Technology, Current Starved Voltage Controlled Oscillator, Performance Analysis, Layout Design.

1. Introduction

In electronics, ensuring oscillators operate efficiently is crucial for numerous devices such as smartphones, laptops, and digital timepieces. This study examines Ring Oscillator (RO) and Current Starved Voltage Controlled Oscillator (CS - VCO) in 90nm CMOS technology. Oscillators serve as the 'heartbeats' of electronic systems, aiding in timekeeping for smartphones, ensuring smooth operations in laptops, and maintaining precision in digital watches. The aim is to comprehend their functionality and optimize performance metrics like speed and power consumption. By comparing different setups, this research seeks to enhance the functionality and speed of electronic devices.

Voltage Controlled Oscillators (VCOs) are fundamental components in modern communication systems, serving critical roles in applications such as clock generation, which is indispensable for various electronic devices. MOSFET - based VCOs present challenges in RF applications due to their inherent characteristics. Power consumption is a significant concern, particularly in RF systems powered by batteries, necessitating careful power optimization techniques. Moreover, technological advancements have driven a trend towards miniaturization, impacting device size and performance.

In a MOS transistor, gate capacitances require a certain charging time before logic level changes can occur, resulting in inherent delay in signal propagation. Utilizing this delay, ring oscillator configurations comprising interconnected inverters can achieve extended delay periods, thereby influencing oscillation frequency. Figure 1 shows the architecture of a typical n - stage ring oscillator.

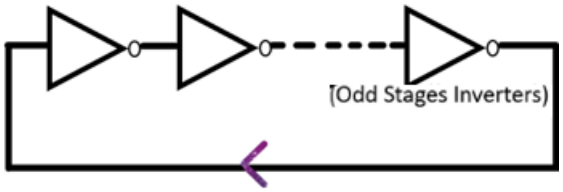

Figure 1: CMOS Ring Oscillator

The cycle period of the Ring oscillator is determined by the time required for signal transition (td), which might be from high to low or low to high, as stated in Equation 1. In this case, N represents the number of connected inverters (also known as delay stages) in the oscillator loop. Due to the existence of two transitions, Equation 1 includes a factor of two (low to high and high to low). But keep in mind that Equation 1 only applies to Equation 3. Equation 2 is thus a suitable notation to represent the oscillation frequency.

$$T = 2 \times N \times t_d \quad (1)$$

$$f_0 = 1/T = 1/2 \times N \times t_d \quad (2)$$

$$2Nt_d >> t_f + t_r \quad (3)$$

Wherein td represents the propagation delay time, N signifies the number of inverters, and f denotes the oscillation frequency. Equation 3 stipulates that the rise and fall time periods, (tr) and (tf), are significantly shorter than the oscillation period (td).

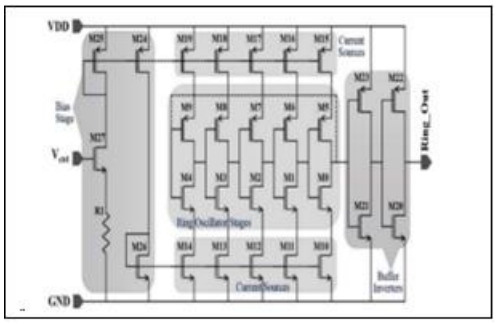

Figure 2: 5- Stage Current Starved VCO

2. Literature Review

The literature survey for this research paper examines previous studies on the performance analysis of Ring Oscillator (CMOS RO) and Current Starved Voltage Controlled Oscillator (CS - VCO) in 90nm CMOS technology. Earlier research has investigated similar aspects of oscillator design and performance, particularly in 180nm technology. By transitioning to the latest 90nm technology, we aim to leverage its advantages for improved efficiency and performance.

Studies on Ring Oscillators have explored the influence of inverter stages on key metrics like delay and frequency, while also proposing optimization strategies for enhanced efficiency. Likewise, research on Current Starved Voltage Controlled Oscillators has focused on design methodologies and performance characteristics unique to CS - VCOs. Comparative studies have evaluated different oscillator configurations, providing insights into their strengths and weaknesses. By building upon existing knowledge and utilizing advancements in technology, this research seeks to contribute to the optimization of oscillator design in semiconductor technology.

3. Circuit Design

a) Current Starved Voltage Controlled Oscillator

In designing the architecture of a Current Starved Voltage Controlled Oscillator (CS - VCO), Three inverters, along with a Pull - Up Network (PUN) and Pull - Down Network (PDN), have been connected in a cascading fashion as part of the architecture design of a Current Starved Voltage Controlled Oscillator (CS - VCO). Whereas the PDN network is built using NMOS transistors, the PUN network consists of PMOS coupled loads. Through the NMOS transistor's gate, a switch known as Vc has been integrated to adjust the frequency.

By varying the voltage given to it, a Current Starved Voltage Controlled Oscillator (CS - VCO) is a kind of oscillator that allows control over its frequency output. Three inverters are placed in a cascading pattern with Pull - Up (PUN) and Pull - Down (PDN) networks in the CS - VCO architecture. Whereas the PDN makes use of NMOS transistors, the PUN is composed of PMOS transistors coupled as loads. This arrangement allows for efficient control of the oscillator's frequency. Additionally, a switch, often referred to as VC, is integrated into the design, enabling further adjustment of the oscillator's frequency by modulating the gate of the NMOS transistor. Overall, the CS - VCO design provides flexibility and precision in frequency control, making it a valuable component in various electronic systems and communication devices.

A Conventional 5 Stage Current Starved Voltage Controlled Oscillator is depicted in the below figure wherein M1, M5, M9, M13, M17 acts as PMOS Current Sources and while M4, M8, M12, M16, M20 acts as NMOS Current Sources in the Circuit diagram shown in Figure 3.

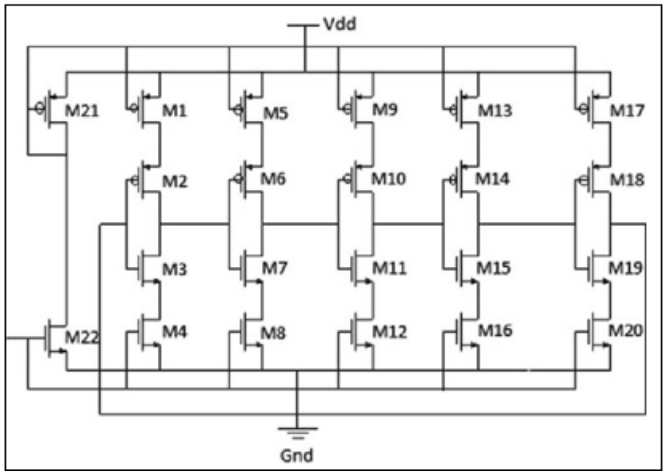

Figure 3: Circuit Diagram of 5– Stage CSVCO

b) CMOS Ring Oscillator

A CMOS Ring Oscillator (RO) is like a string of light switches connected in a loop. Each switch takes some time to turn on and off. When they're all connected together, they keep flipping back and forth, making a signal that goes on and off. To make one, we just need to put a bunch of these switches, called inverters, in a circle. By choosing how many inverters to use and how fast they turn on and off, we can make the signal go faster or slower.

For the CMOS Ring Oscillator, we're experimenting with different setups using various numbers of inverters, such as 3, 5, and 7 stages. Imagine each inverter as a building block in a chain, and by connecting them in loops of different lengths, we can create oscillators with different frequencies. This way, we can see how the number of stages affects the performance of the ring oscillator and find the best setup for our purposes. A typical 5 stage CMOS Ring Oscillator is shown in the figure 4.

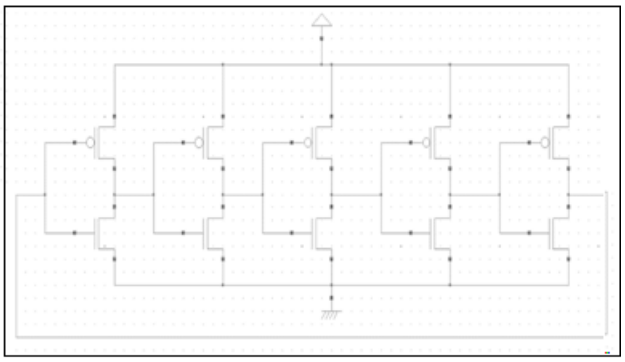

Figure 4: Circuit Diagram of 5 - Stage CMOS Ring Oscillator

Now in the next section we'll analyze various responses and parameters like Transient Response, Delay, Frequency and Power. Power efficiency is paramount across all electronic systems, but it becomes especially critical in RF applications powered by batteries. These systems demand meticulous attention to detail to minimize power dissipation and extend operational life.

4. Experimental Findings and Analysis

In this section, we present the simulated results obtained from our experiments with both CMOS Ring Oscillator (RO) and Current Starved VCO (CS - VCO) designs. The simulations were conducted using Industry standard software tools like Cadence Virtuoso for Design and Simulation and Microwind for layout design to analyse the performance characteristics of each oscillator configuration.

a) Current Starved VCO (5 - Stage)

For the CS - VCO, we investigated the impact of voltage control on the oscillator's frequency and the variation of power. By adjusting the voltage applied to the oscillator circuit, we observed changes in the oscillation frequency and stability. Additionally, we analysed the influence of other parameters, such as the delay, frequency, power and transistor characteristics, on the overall performance of the CS - VCO.

The Design Parameters for CS - VCO 5 – stage shown in figure 4 are depicted below:

Table 1: Design Parameters for 5 – Stage CS – VCO

Design Parameters for CS-VCO				
Transistors	M1, M9, M13, M17, M5, M21	M2, M14, M6, M10, M18	M3, M15, M19, M7, M11	M12, M4, M8, M16, M20
W/L	5	4.4	2.2	1.7

The designed circuit diagram for the 5 – stage Current Starved Voltage Controlled Oscillator in Cadence Virtuoso design tool is illustrated in Figure 5.

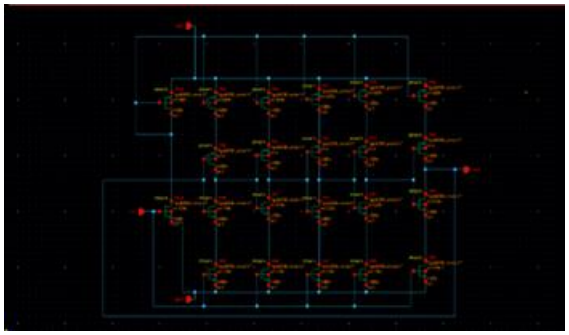

Figure 5: Circuit Design

The Transient response (Voltage (v) vs the Time (ns)), Frequency Response (Frequency (GHz) vs Voltage (v)) and Parametric Analysis (For various voltages) obtained for the designed circuit are shown in Figures 6 & 7.

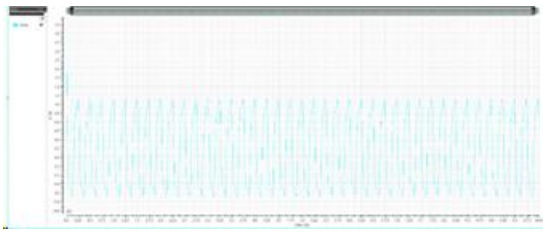

Figure 6: Transient Response

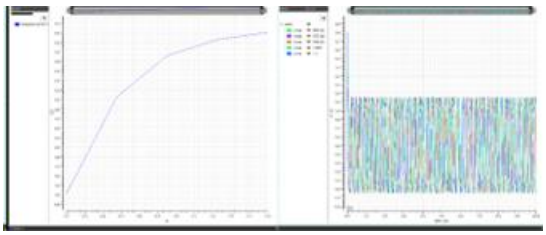

Figure 7: Frequency Response and Parametric Analysis.

Based on the analysis of the Current Starved - VCO (CS - VCO) 5 - stage design conducted using Cadence Virtuoso software with GPDK 90nm library, we achieved a frequency range of 1.02 to 4.4 GHz by varying the voltage applied to the oscillator circuit from 0.4V to 1.5V. Furthermore, we estimated the power consumption of the CS - VCO design to be within a certain range based on previous power consumption analysis and considering the voltage and frequency ranges tested. The maximum power consumption was found to be 1.25 mW.

In conclusion, the CS - VCO 5 - stage design demonstrated a wide frequency range of operation, spanning from 1 GHz to 4.4 GHz, making it suitable for various applications requiring different operating frequencies. Additionally, the maximum power consumption of 1.25 mW indicates reasonable power efficiency across the operational range. These results underscore the CS - VCO's effectiveness and versatility in meeting the requirements of modern semiconductor applications.

b) CMOS Ring Oscillator (3, 5, 7 Stage)

For the CMOS Ring Oscillator, we varied the number of inverters in the loop, including setups with 3, 5, and 7 stages. Our analysis focused on key parameters such as frequency, delay, and power consumption. By comparing the results

from different setups, we aimed to identify the optimal configuration for achieving the desired performance metrics.

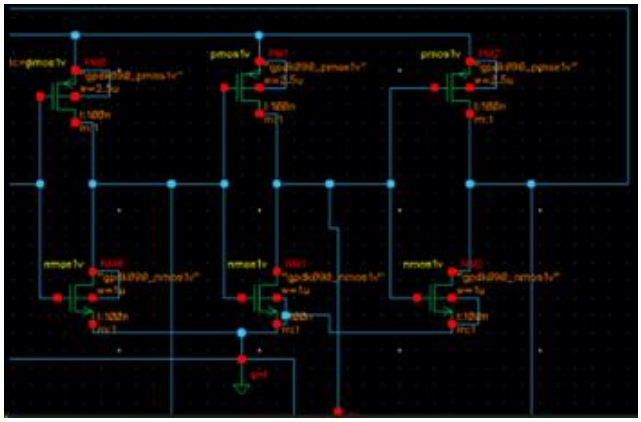

Figure 8: Circuit Diagram (3 – Stage)

The Layout design of Current Starved VCO (5 - stage) and CMOS Ring Oscillator (3, 4, 7 Stage) for Physical implementation and spatial arrangement of components in these advanced semiconductor technologies are dipicted in the Figures 9, 10 & 11.

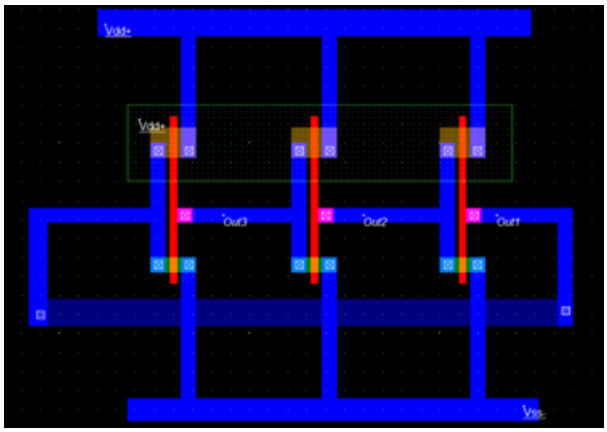

Figure 9: Layout of 3–Stage CMOS Ring Oscillator

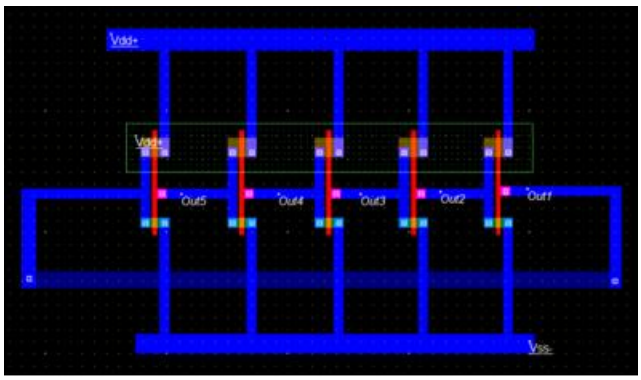

Figure 10: Layout of 5–Stage CMOS Ring Oscillator

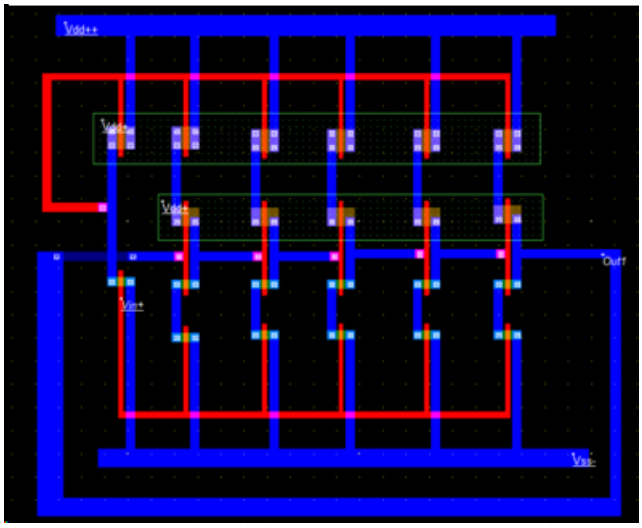

Figure 11: Layout of 5–Stage Current Starved VCO

The Power Analysis of CMOS Ring Oscillator and 5 - Stage CSVCO is shown below:

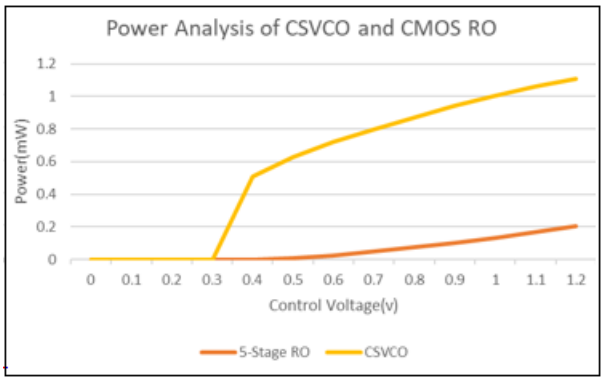

Figure 12: Power Analysis of CSVCO and CMOS RO

The Power parameter variations depicting the influence of altering numbers of Inverter stages in the CMOS Ring Oscillator is shown in Figure 13.

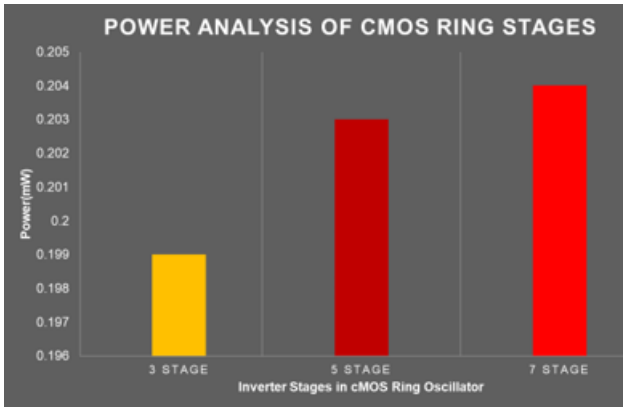

Figure 13: Power Analysis of CMOS RO

The complete analysis for CSVCO based on previous works and analysis is shown in below table.

Table 2: Performance Comparison of CSVCO

Design Reference Number	Technology Node(nm)	No. of Stages	Control Voltage(v)	Output Frequency Range(GHz)	Power Dissipation (mW)
[1]	180	3	2.5	5	13.5
[2]	90	2	1.5	1.22-3.22	9.61
Proposed work	90	5	0.4-1.5	1.02-4.4	1.2

5. Conclusion

In this paper, we conducted a comparative analysis between two oscillator topologies, namely the Ring Oscillator (CMOS) and the Current Starved VCO (CSVCO), within the context of existing literature, utilizing the 90 nm CMOS technology node. Our investigation focused on Assessing factors like delay, frequency, and power consumption to enhance oscillator efficiency. Through simulation results, We noticed that elevating the control voltage enables higher oscillation frequencies, showcasing CSVCO's broad frequency span from 1.12 to 4.4 GHz, with power usage recorded at 1.2 mW within a control voltage range of 0.4 to 1.5V. Conversely, the CMOS Ring Oscillator displayed a decline in frequency with an increase in the number of inverter stages, coinciding with a surge in power consumption.

Although CSVCO presented a broader frequency range, it also exhibited higher power consumption compared to the CMOS Ring Oscillator. Therefore, while CSVCO offers a wider frequency range, its higher power consumption favors the CMOS Ring Oscillator as the more efficient choice, particularly for applications emphasizing power efficiency.

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