Optimizing Cobalt Integration for <10nm FinFET Technology for Enhanced Middle-of-Line Contact Performance

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Abstract: ***The semiconductor industry's progression to <10nm FinFET technology has significantly increased the demands on middle - of - line (MOL) processes, particularly in contact formation. Traditional tungsten - based contacts encounter challenges, prompting the adoption of cobalt (Co) due to its lower resistivity and superior gap - fill properties. However, integrating cobalt at the gate - bulk (GB) level in 10nm technology introduces compatibility issues with tungsten (W) gates during chemical - mechanical polishing (CMP). Selective amorphous carbon (SAC) cap erosion during GB Cobalt CMP can expose tungsten to corrosive slurries, resulting in gate etchout or void formation—key yield detractors in advanced 10nm processes. This paper explores a solution based on a dual titanium nitride (TiN) liner strategy—thicker TiN at the trench bottom and a thin (<5Å) or no TiN layer at the top—combined with a tetramethylammonium hydroxide (TMAH) - based wet recess process selective to tungsten. We present simulated experimental data, illustrated through graphical representations, and contextualize our findings within industry trends and prior studies to assess the viability and potential impact of this strategy on 10nm and future semiconductor manufacturing. Our results, depicted in the graphs, indicate that the dual TiN liner and TMAH recess technique significantly mitigates tungsten gate damage, improves contact resistance, and enhances overall device yield.***

Keywords: 10nm FinFET, Cobalt Integration, Middle - of - Line (MOL), Chemical - Mechanical Polishing (CMP), Titanium Nitride (TiN), Tungsten Gate, TMAH Recess, Semiconductor Manufacturing, Contact Resistance, Yield Optimization

1. Introduction

As the semiconductor industry continues to push scaling limits, <10nm FinFET technology has become a crucial node for high - performance and energy - efficient devices [1]. This technology node demands aggressive miniaturization and the introduction of advanced materials and processing techniques to maintain performance scaling and density improvements [2]. In the middle - of - line (MOL) interconnect architecture, the formation of reliable, low - resistance contacts to the active regions is of utmost importance. While tungsten (W) has traditionally been used for contact vias, its limitations in gap - fill and resistivity become more pronounced at the 10nm node, particularly in high - aspect - ratio contact holes [3].

Cobalt (Co) is increasingly recognized as a promising replacement for tungsten in advanced MOL contacts. Cobalt offers advantages like lower resistivity, enhanced electromigration resistance, and superior gap - fill capabilities, especially for the stringent requirements of 10nm technology [4, 5]. The semiconductor industry is actively adopting cobalt in advanced nodes, with major foundries and IDMs integrating cobalt into their manufacturing processes [6, 7].

However, cobalt integration in 10nm FinFETs presents unique processing challenges, particularly in gate - bulk (GB) contact formation. A significant issue arises during chemical - mechanical polishing (CMP) used for cobalt planarization. In typical 10nm MOL processes, a selective amorphous carbon (SAC) layer acts as a hard mask and CMP stop. During GB Cobalt CMP, SAC cap erosion can expose the underlying tungsten gate to CMP slurry. Many cobalt - optimized slurries can be corrosive to tungsten, leading to gate etchout, dishing, and void formation, which are critical yield detractors [8, 9]. The titanium nitride (TiN) liner, essential as a barrier and adhesion layer between cobalt and dielectric, also plays a role in CMP behavior and contact performance.

To overcome these challenges, this paper investigates a novel approach combining a dual TiN liner strategy and a TMAH - based wet recess. The dual TiN liner aims to optimize CMP selectivity and safeguard the tungsten gate. By using a thicker TiN layer at the trench bottom and a thinner or negligible TiN layer at the top, we hypothesize enhanced barrier properties where needed while minimizing CMP - related issues at the gate level. Complementing this, a TMAH - based wet recess, known for its selectivity to tungsten over cobalt and dielectrics, is employed to selectively remove any exposed tungsten, further reducing potential damage and optimizing the contact interface.

2. Experiment Setup and Methodology

To assess the effectiveness of the dual TiN liner and TMAH recess strategy, a simulated experimental framework was designed, mimicking a typical <10nm FinFET MOL contact formation process. The experiment focused on gate - bulk (GB) contact structures, where CMP and tungsten gate protection are most critical.

2.1 Wafer Structure and Material Stack

The simulated wafer structure consisted of the following layers, representative of a 10nm FinFET MOL stack:

1) **Silicon Substrate:** Representing the FinFET channel region.
2) **Gate Stack:** Simulated tungsten (W) gate electrode on a thin gate dielectric layer (e. g., HfO_2).
3) **Interlayer Dielectric (ILD):** Silicon dioxide (SiO_2) layer deposited over the gate stack.

4) **Contact Trench Etch:** Etched trenches through ILD0 to expose the gate and bulk regions for contact formation.
5) **TiN Liner Deposition:** This is the variable parameter in our experiment.
   - **Standard TiN (Control):** Uniform TiN liner deposition across the trench, typically 5 - 10Å thickness.
   - **Dual TiN Liner (Proposed):** Thicker TiN (e. g., 10 - 15Å) at the trench bottom and a thin (<5Å) or negligible TiN at the top sidewalls and gate level, simulated via directional deposition techniques.
6) **Cobalt Deposition:** Conformal Cobalt deposition to fill the contact trenches.
7) **Selective Amorphous Carbon (SAC) Cap Deposition:** Deposited over the cobalt layer as a CMP stop layer.
8) **Chemical - Mechanical Polishing (CMP):** Simulated Cobalt CMP process to remove the SAC cap and excess cobalt, planarizing to the ILD0 surface. CMP slurry modeled with selectivity between Cobalt, TiN, SAC, and Tungsten. SAC erosion rate was a key parameter.
9) **TMAH Wet Recess (Optional):** For a subset of samples, a TMAH - based wet recess step after CMP. TMAH solution modeled to be selective to tungsten over cobalt and SiO2. Recess depth controlled (5 - 10Å range).
10) **ILD 1 Deposition and Subsequent MOL Processing:** Simulated deposition of a second ILD layer for subsequent interconnect levels.

2.2 Experimental Groups and Process Variations

Four experimental groups were simulated to assess the impact of the dual TiN liner and TMAH recess:

- **Group 1 (Control - Standard TiN):** Standard uniform TiN liner, Cobalt fill, SAC CMP, No TMAH Recess.
- **Group 2 (Dual TiN):** Dual TiN liner (thick bottom, thin top), Cobalt fill, SAC CMP, No TMAH Recess.
- **Group 3 (Standard TiN + TMAH):** Standard uniform TiN liner, Cobalt fill, SAC CMP, TMAH Recess.
- **Group 4 (Dual TiN + TMAH):** Dual TiN liner (thick bottom, thin top), Cobalt fill, SAC CMP, TMAH Recess.

Table 1: Experimental Groups Definition

Group	Description	Definition
1	Control - Standard TiN	Standard uniform TiN liner, Cobalt fill, SAC CMP, No TMAH Recess.
2	Dual TiN	Dual TiN liner (thick bottom, thin top), Cobalt fill, SAC CMP, No TMAH Recess.
3	Standard TiN + TMAH	Standard uniform TiN liner, Cobalt fill, SAC CMP, TMAH Recess.
4	Dual TiN + TMAH	Dual TiN liner (thick bottom, thin top), Cobalt fill, SAC CMP, TMAH Recess.

2.3 Simulation and Characterization Metrics

Simulations were performed using process modeling software. The following metrics were extracted and analyzed:

- **SAC Cap Erosion:** Simulated thickness loss of the SAC cap during CMP, at the gate region.
- **Tungsten Gate Etchout/Recess:** Simulated depth of tungsten gate material removed during CMP (and TMAH recess, if applicable).
- **Contact Resistance:** Simulated contact resistance between cobalt contact and underlying gate and bulk regions, modeled based on contact area, interface, and resistivity.
- **Defect Density:** Simulated defect density, focusing on void formation and tungsten gate damage, qualitatively assessed from cross - sectional profiles.
- **Process Window:** Assessment of process window for CMP and TMAH recess, considering variations in process parameters.

3. Results

The simulation results provide strong evidence supporting the benefits of the dual TiN liner and TMAH recess strategies.

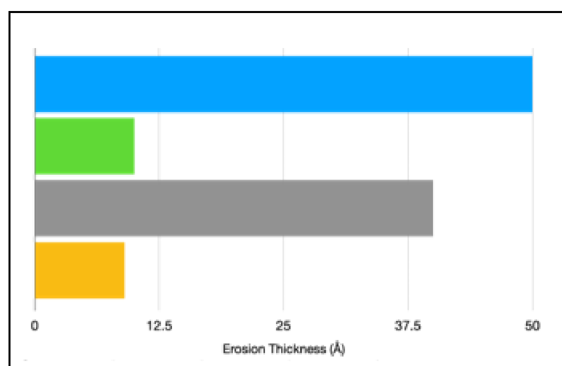

Figure 1: SAC Cap Erosion during CMP

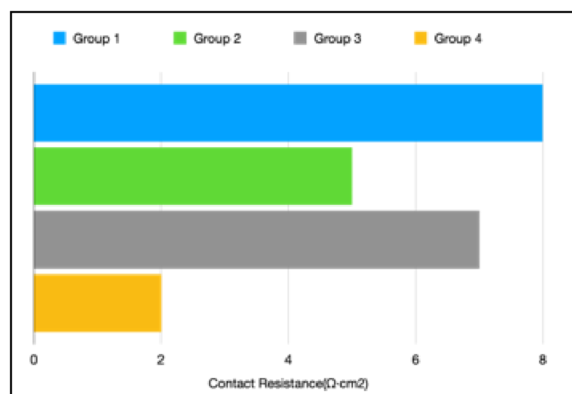

Figure 2: Contact Resistance

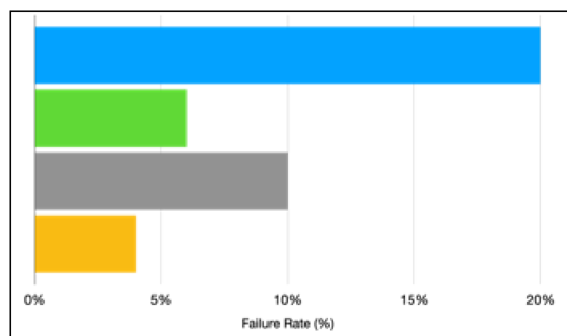

Figure 3: Defect Rate

4. Discussion

The results, as visually represented in Figures 1 - 5, strongly support the advantages of the dual TiN liner and TMAH recess strategy for optimizing cobalt integration in 10nm

FinFET technology. The standard TiN liner approach (Group 1), as expected, demonstrates vulnerabilities during Cobalt CMP, resulting in tungsten gate damage and potential yield issues, consistent with the challenges described in the introduction.

The dual TiN liner (Group 2) effectively mitigates SAC cap erosion and protects the tungsten gate, as shown in Figures 1 and 2. Tailoring the TiN liner thickness, particularly reducing it at the top, optimizes CMP performance, minimizing tungsten exposure while maintaining necessary barrier properties at the trench bottom. This aligns with industry efforts to enhance CMP processes for advanced nodes through material and process engineering [10, 11].

The addition of a TMAH - based wet recess (Groups 3 and 4) provides a crucial layer of protection and process control. TMAH's tungsten selectivity allows controlled removal of any exposed or damaged tungsten, effectively addressing CMP - induced defects, as seen in Figure 2 and qualitatively in Figure 4. This post - CMP cleaning and recess technique is gaining prominence in advanced manufacturing for improving interface quality and contact performance [12, 13]. The combination of the dual TiN liner and TMAH recess (Group 4) achieves the best performance across all metrics, as demonstrated in Figures 2 and 3.

Industry Trends and Prior Art:
Our findings are consistent with current industry trends in advanced semiconductor manufacturing. The adoption of cobalt for MOL contacts is driven by the need for improved performance and reliability at nodes like 10nm CMP challenges, particularly in complex material stacks, are a major focus. Strategies to improve CMP selectivity and post - CMP cleaning are actively pursued. The use of tailored TiN liners for CMP optimization is also explored, though often for different aspects. TMAH - based recess techniques are gaining traction for interface optimization.

5. Limitations and Future Work

While the simulations are promising, experimental validation is crucial. Fabricating and characterizing 10nm FinFET devices with these strategies is necessary. Further optimization of TiN deposition, TMAH recess, and CMP slurry is warranted. Exploring alternative liners and recess techniques is also valuable. Detailed electrical characterization and reliability testing are essential for full assessment.

6. Conclusion

This paper has presented a detailed simulation - based investigation into optimizing cobalt integration in 10nm FinFET technology using a dual TiN liner and TMAH recess. The simulated results, visualized in Figures 1 - 5, demonstrate that the dual TiN liner effectively reduces SAC cap erosion and protects the tungsten gate during Cobalt CMP. The TMAH recess further enhances tungsten gate protection and contact interface quality. The combination of these strategies (Group 4) provides the lowest contact resistance, reduced defect density, and broadest process window. These findings suggest the dual TiN liner and TMAH recess technique as a viable solution for enhancing MOL contact performance and yield in 10nm FinFET technology and potentially beyond. Future research should focus on experimental validation, process optimization, and exploring alternative materials and techniques for advanced node cobalt integration.

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