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Implementation of Low Power Ternary Logic Gates using CMOS Technology

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Abstract: ***This paper describes the architecture, design & simulation of ternary logic gates. In a VLSI circuit, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to devices [1]. The binary logic is limited due to interconnect which occupies large area on a VLSI chip. In this work, the designs of ternary-valued logic circuits have been explored over multi-valued logic. The proposed GATES are designed & simulated with the help of Microwind EDA tool's. These Gates are implemented using C-MOS ternary logic (T-Gates) The new family is based on CMOS technology and is thus open to VLSI implementation. The proposed design is comprised of a set of inverters, NOR gates, and NAND gates. The designed technique used here requires the width and length calculations of the CMOS gates to improve the design. The proposed logic can be implemented at its layout side using 45 nm technologies.***

Keywords: Ternary, Multi valued logic, CMOS, VLSI

1. Introduction

Because of the advanced MOS technology & an easily implemented binary algebra, the circuit complexity of binary logic has been successfully pushed to the VLSI/ULSI level. However, there exists some problem in present-day binary systems that of interconnection, both on chip and off chips. On chip, the interconnection problem is in the wire routing. As the scale of integration continues to increase, the silicon area for wire routing becomes increasingly greater than that for the active logic elements, owing to the vast information exchanges between each active block in the system. Therefore the speed of a circuit decreases, due to the accompanied larger capacitance with the longer interconnection lines. In the other respect, the interconnections between chips face the pin number limit. As well as the pin counts increasing at an incredible rate as the chip becomes larger, the system performance is also sacrificed due to frequent off-chip connections. All the above difficulties can be reduced if the information content per interconnection is raised from the present binary level to multilevel by multivalued logic, to reduce the burden of interconnection. Multivalued logic therefore becomes quite attractive in VLSI/ULSI development, due to its potential advantages over binary logic for designing of digital systems [1] [2] [3]. Compared to binary logic, ternary logic allows more information to be transmitted over a given set of lines thus reducing the chip size area. Thus it is more effective way of utilizing interconnections by using a larger set of signals over the same area in multiple-valued logic (MVL) circuits. This also solves the problem of pin out & because of less estimation interconnection cost it receives more attention [4].

Commercially multiple-valued logic have made an appearance for implementing the circuits like multi valued logic memories The circuits using ternary logic are theoretically more economical than the ones using binary logic [5][6]. The main draw back in multiple valued logic circuits is that their design techniques are more complex than the binary logic circuits. The implementation of MVL circuits have ranged through integrated injection logic, emitter coupled logic, CMOS and n-MOS technologies and charge-coupled devices.

Several authors [7-12] have used CMOS integrated circuits for the realization of three-valued logic circuits. These designs have used power supply voltages higher than the MOSFETs threshold voltage which resulted in high power consumption in the circuits. Mouftah and Smith [13] have reported a family of low power three- valued CMOS circuits. The design of simple ternary inverter (STI) is based on use of a CMOS inverter. In design of positive ternary inverter (PTI), negative ternary inverter (NTI) we can use a pass transistors/CMOS transmission gate at its output.

2. Design and Simulation of Ternary Logic Gates

The most fundamental building blocks in the design of digital systems are the inverter, NOR gate, and NAND gate. We propose the ternary implementations for the inverter, NOR gate, and NAND gate. The prime objective in our work is to minimize the number of transistors used, eliminate the use of resistors to lower the power consumption, reduce the propagation delay time. The reduction in the number of transistors is our main focus as that enabled a more compact design which utilized the less chip area.

3. Ternary Inverter

The ternary inverter is a complement function; which in the binary notation is known as an inverter. It is also called as the MVL-NOT function. There are three basic ternary elements: the STI (Simple Ternary Inverter), the NTI (Negative Ternary Inverter) and the PTI (Positive Ternary Inverter), whose logic functions are shown in Tab. 1. The rule of ternary inversion for these three types of basic ternary operations are defined by

$$Xc = \begin{cases} C & if\ x = 1 \\ C - X, & if\ x \neq 1 \end{cases}$$

C in above equation takes the values of logic 2 for a PTI, logic 1 for a STI and logic 0 for a NTI which correspond to higher level (2), middle level (1) and lower level (0), respectively. A MVL-NOT function is an elementary function in MVL. In order to make a voltage mode multi-valued signal, high accuracy is necessary, because the voltage levels for each logic level are an equal division of VDD.

Table 1: Truth table for Ternary Inverter

X	*NTI*	*PTI*	*STI*
0	2	2	2
1	0	2	1
2	0	0	0

The logic symbols of these three inverters are given in figure 1.

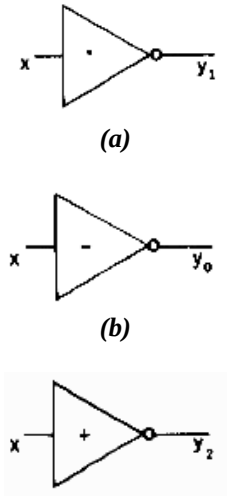

Figure 1: T- inverter symbols (a) STI. (b) NTI (c) PTI

3.1 Design of STI

Fig.2 shows design layout of a Simple Ternary Inverter (STI) implemented using a PMOS transistor & NMOS transistor with Logic 2 at VDD, Logic 0 at GND (0 V) & logic 1 is a middle voltage between VDD & GND. The resistance of channels can be change by altering the length-to-width ratio of the PMOS and NMOS channels. Thus, the resistance of the circuit is directly proportional to its L/W ratio which can be effectively used to change the resistance of transistors to suit design needs [8] [9].

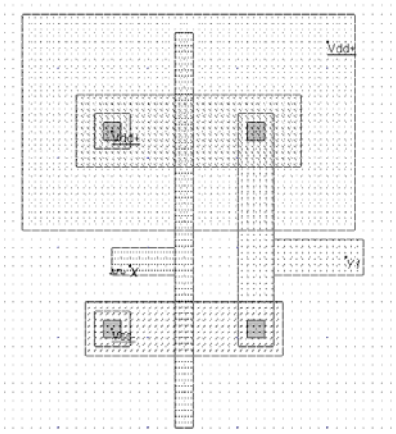

Figure 2: Layout of Standard Ternary Inverter (STI)

These elements form a complete set of algebraic operators and more complex ternary functions, as the TNAND (Ternary NAND) and TNOR (Ternary NOR), can be realized by using them. The circuit operation of this STI is simulated & analyzed on microwind. Figure 4 shows the output Voltage Vs Time characteristics. Table 2 gives the logic level voltages for inputs and outputs of STI.

Table 2: STI Logic Level Voltage

Logic Value	*Voltage Level I/p (V)*	*Voltage Level O/p (V)*
0	0	1.0
1	0.5	0.51
2	1.0	0

The power dissipation and the transition time of output voltage signal are observed to be very small as specified in result section.

4. Design of Ternary NAND gate

A TNAND function gives the inversion of the minimum value of the input signal where input signal belongs to 0, 1 and 2 or -1, 0 & +1 in balance ternary. The NAND o/p can be defined as

Y= INV [Min (I1,I2,I3…...In)]

The truth table of the function is given in Table 3

Table 3: Ternary NAND truth table

Input A	*Input B*	*O/P TNAND*
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

The CMOS design of proposed TNAND gate is shown in figure 3. The results of the design are simulated on Micro wind. Fig 5 shows the result of the Voltage Vs Time for the different input logic levels.

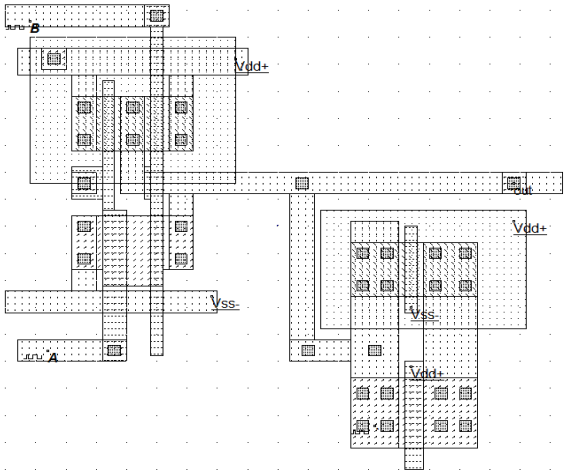

Figure 3: Layout of TNAND

5. Design of Ternary NOR gate

A TNOR o/p function gives the inversion of the maximum value of the input signal. Thus the NOR o/p can be defined as;

Y= INV [Max (I1,I2,I3…...In)]

The truth table for this function is given in Table 4

Table 4: Ternary NOR truth table

Input A	*Input B*	*O/P TNOR*
0	0	2
0	1	1
0	2	0
1	0	1
1	1	1
1	2	0
2	0	0
2	1	0
2	2	0

The CMOS design of proposed TNOR gate is shown in figure 4. The results of the design are simulated on Micro wind. Fig 6 shows the result of the Voltage Vs Time for the various input logic levels. The output is verified as per the truth table.

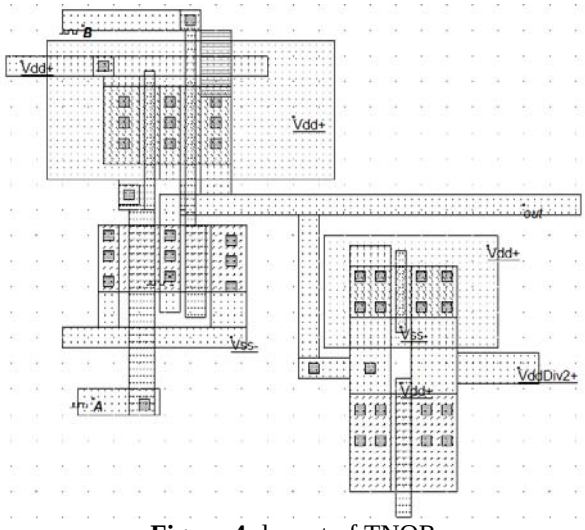

Figure 4: layout of TNOR

6. Results and Discussions

Design of the Standard Ternary Inverter, Ternary NAND & Ternary NOR are verified and analyzed for their output voltage characteristics using Microwind with 45 nm technology. Figure shows the output voltage Vs Time characteristics for these designs.

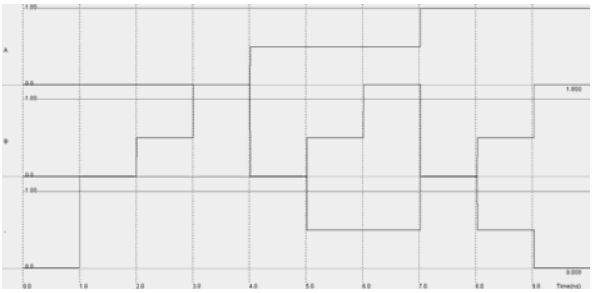

Figure 5: Output Voltage Vs Time characteristic for STI

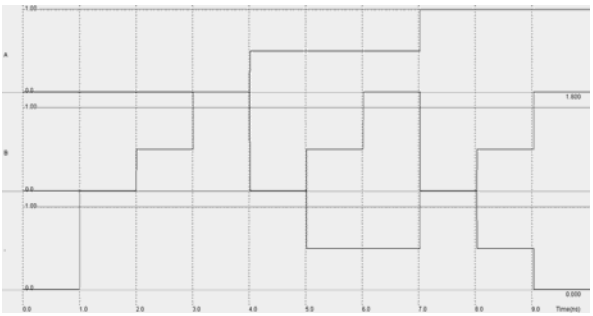

Figure 6: Output Voltage Vs Time characteristic of TNANAD

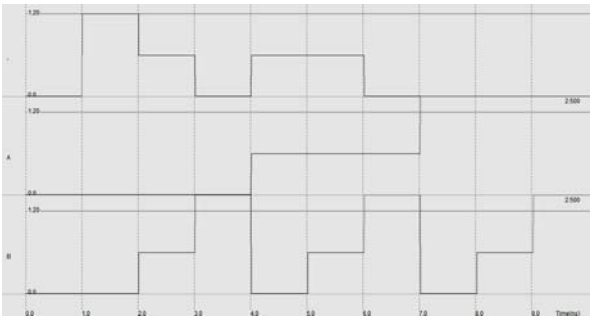

Figure 7: Output Voltage Vs Time Characteristic of TNOR

The outputs of all these gates are verified for the respective truth table. The designs are proposed with the minimum transistor count thereby reducing the overall power dissipation and reducing the transition times.

Table 5 shows the on screen power dissipation over 500 ns time scale associated with the respective logic gate.

Table 5: Power Dissipation

Gate	*Power Dissipation*
STI	0.19 µW
TNAND	0.17 mW
TNOR	0.167 mW

The transition time of inverter is found to be 2.75 ns & is considered to be very small as compared with given in references.

7. Conclusion

In most of the traditional designs, the transmission gates are use to pull the output to specific required voltage. In this proposed design the output transmission gate is eliminated thereby reducing the component count which leads to significant reductions in the overall power dissipation and improving the transition time. The proposed logic gates are useful further to design the low power ternary circuits. Considering the various advantages of the multi valued logic, the appropriate design of the MVL logic gates is important so that it will lead to the further development and its applications in this area.

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