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A CMOS Current-Mode Full-Adder Cell for Multi Valued Logic VLSI

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Abstract: ***The thesis describes the design and implementation of a carry save adder cell for multi-valued logic VLSI. A four-valued system was chosen and the logic was analysed and minimized using the C HAMLET CAD tool [I]. SPICE was used to design and simulate the required behaviour of the current-mode CMOS circuits. A VLSI test and evaluation integrated circuit was implemented with MAGIC and fabricated through the MOSIS service. The completed IC was tested and evaluated using a specially designed binary-to multi- valued logic converter and decoder. Engineering modifications to the original current-mode inverter cells used by HAMLET were made leading to significant power savings in a complete design. The fabricated device performed as predicted by SPTCE simulation. Exhaustive functional testing produced correct steady-state output signals for all cases of input loadings. Finally, we show HAMLET minimization heuristics are not efficient in the design of adder cells by comparison with an alternative modulo 4 carry save adder cell in current-mode CMOS.***

Keywords: CMOS, CAD, SPICE, HAMLET

1. Introduction

In recent years, continued improvements in VLST fabrication processes have led to a renewed interest in current-mode CMOS high-radix arithmetic circuits. Of particular importance is the development of high speed compact multiplier circuits for the rapidly expanding fields of digital signal processing and digital control systems. The most modern high-speed arithmetic units, multiplication of long data words is performed by simultaneously generating sets of partial products and then summing them together with a network of carry save adders (CSAs) in an operation that is referred to as "row reduction." Although the network of CSAs lends itself very well to pipelining in high-speed processors, binary multipliers using the Wallace Tree [6J approach suffer from scalability problems Scalability difficulties can be overcome by utilizing a high-radix signed number system to significantly reduce the number of transistors and the die area required for large data-word arithmetic Presently, current-mode CMOS logic is not a simple solution for the generation of partial products in a large multiplier circuit. One alternative is to use binary CMOS circuits to implement a modification of Booth's algorithm[2]. However, the design of high-radix adders lends itself well to current “mode CMOS, primarily because of the wired sum [3] function. One of the key elements of the adder circuit is the threshold detector [4]. This particular circuit has, in the past, proved to be difficult to scale down to minimum VLSI implementation device sizes. With the vast and continuing improvements in CMOS fabrication processes, this design problem can be minimized. Of recent interest is the development of alternative low-power high-speed threshold detector circuits such as those found in CML current-mode full adders[5]

In this thesis we demonstrate the design and implementation of a radix-4, carry-save adder cell for multi-valued VLSI, The adder receives current inputs X. Y, and Carry IN generating the Sum and Carry OUT outputs. The Carry lN input of the carry save adder accepts all possible radix-4 inputs (0:3) so that it may be used as a three-to-two row reduction unit in the CSA adder network previously described.

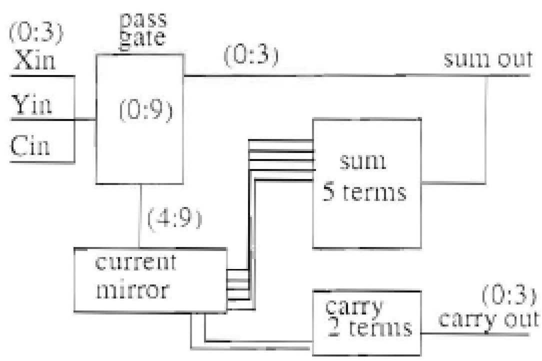

Figure 1: Block Diagram of New 'Modulo 4 adder

2. HAMLET - A CAD Tool for MVL Design

To realize a logic function in multi-valued log (MVL), a design method is required to develop the abstraction into a format on which CAD tools can perform heuristics. Unlike binary logic design, MVL of radix greater than 2 quickly becomes difficult to conceptualize. For example, while a two-input NAND gate is readily described in binary logic, there is no "symbol" to functionally describe a two-input NAND gate in a logic system of 6 variables. The MVL CAD tool HAMLET uses a sum-of 'products (SOP) expression as formatted input D. Since HAMLET will minimize the SOP expression, any valid SOP expression which completely describes the functionality of the design is sufficient. The SOP is derived from a mapping technique which resembles the familiar Karnaugh Map method. Let X = {*x1.x2* •.... _"*xn* } be a set of variables in a logic system of radix r, where *x1* takes on values from R = {O, I,2, . ..,r-l).

3. Minimization of' Literals Using Hamlet Heuristics

Once the file containing the required SOP terms was input into the HAMLET CAD tool, a report was generated which returned the original expression with matrices representing the mappings for the sum and carry functions. Two heuristic Minimization techniques were chosen to minimize the terms required for this design_ The first was the Deuck & Miller and Proper & Annstrong heuristics[l]. This technique resulted in a reduction from 48 to 32 terms required for the sum function, and from 17 10 15 terms required to realize the carry function. Simulated Annealing minimization was also used, and HAMLET reported the same performance. In each case, the tool verifies each minimization by producing the mappings associated with each result. Copies of all HAMLET generated reports and a copy of the input data file are included in the appendix. Table 1 and Table 2 give the reduced SOP expressions returned by HAMLET which were utilized to implement the modulo-four adder. The reduced SOP expression generated by HAMLET for the sum function'

Table 1: Reduced SOP for Sum Function

1 * x1(3,3) * x2(0,1) * x3(3,3)	+ 1 * x1(3,3) * x2(2,3) * x3(0,0)
+ 1 * x1(3,3) * x2(0,2) * x3(2,2)	+ 3 * x1(2,2) * x2(1,1) * x3(0,0)
+ 2 * x1(0,1) * x2(0,0) * x3(2,2)	+ 1 * x1(0,1) * x2(3,3) * x3(2,3)
+ 1 * x1(2,3) * x2(3,3) * x3(0,0)	+ 2 * x1(0,0) * x2(3,3) * x3(0,0)
+ 1 * x1(1,1) * x2(0,0) * x3(0,2)	+ 1 * x1(3,3) * x2(3,3) * x3(3,3)
+ 2 * x1(0,0) * x2(2,2) * x3(1,1)	+ 1 * x1(3,3) * x2(1,3) * x3(1,1)
+ 1 * x1(2,3) * x2(1,2) * x3(2,2)	+ 3 * x1(1,1) * x2(2,2) * x3(0,0)
+ 1 * x1(1,3) * x2(3,3) * x3(1,1)	+ 1 * x1(1,1) * x2(2,3) * x3(2,3)
+ 1 * x1(2,3) * x2(0,1) * x3(3,3)	+ 2 * x1(2,2) * x2(0,0) * x3(0,0)
+ 3 * x1(0,0) * x2(1,1) * x3(2,2)	+ 2 * x1(1,1) * x2(1,1) * x3(0,1)
+ 3 * x1(2,2) * x2(2,2) * x3(3,3)	+ 3 * x1(0,0) * x2(0,0) * x3(3,3)
+ 1 * x1(0,1) * x2(2,3) * x3(3,3)	+ 3 * x1(2,2) * x2(3,3) * x3(2,2)
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+ 3 * x1(2,2) * x2(0,0) * x3(1,1)	+ 1 * x1(0,1) * x2(0,1) * x3(1,1)
+ 1 * x1(0,0) * x2(2,3) * x3(0,0)	+ 1 * x1(0,0) * x2(1,2) * x3(0,1)
+ 1 * x1(2,3) * x2(2,3) * x3(1,1)	+ 1 * x1(2,3) * x2(2,2) * x3(2,2);

The reduced SOP expression for the carry function is:

Table 2: Reduced SOP for Carry Function

1 * x1(2,2) * x2(0,1) * x3(2,3)	+ 1 * x1(2,2) * x2(1,1) * x3(1,1)
+ 1 * x1(1,1) * x2(2,2) * x3(1,1)	+ 1 * x1(0,2) * x2(3,3) * x3(1,2)
+ 1 * x1(0,2) * x2(2,2) * x3(2,2)	+ 1 * x1(3,3) * x2(3,3) * x3(2,2)
+ 1 * x1(3,3) * x2(1,3) * x3(0,0)	+ 1 * x1(1,2) * x2(3,3) * x3(0,0)
+ 1 * x1(0,0) * x2(1,3) * x3(3,3)	+ 1 * x1(1,1) * x2(1,1) * x3(2,2)
+ 1 * x1(3,3) * x2(0,3) * x3(1,3)	+ 1 * x1(1,3) * x2(2,3) * x3(3,3)
+ 1 * x1(2,2) * x2(2,2) * x3(0,1)	+ 1 * x1(2,2) * x2(3,3) * x3(3,3);
+ 1 * x1(1,1) * x2(0,1) * x3(3,3)	

4. Implementation

4.1 Current-Mode CMOS Logic

To implement the MVL expression, Current-Mode CMOS was utilized. in essence, different values of current correspond to the four different logic levels. A serious drawback to this implementation is that it requires current to be constantly flowing in the circuit. The logic levels and switching point. were designed as shown in figure 2 Currents are shown above are in µA

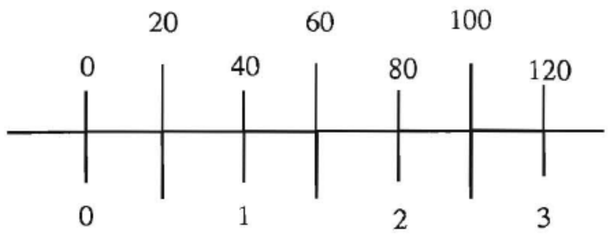


Figure 2: Current Logic Levels

4.2 Limitations of the Present CAD Tool - HAMLET

During the implementation phase of the radix-4 adder, certain limiting features of HAMLET were discovered and re-engineered using the current MOSIS 2.0 micron design rules A program created by KO[4] in support of the HAMLET project generates a PLA in current mode CMOS when given an MYL SOP expression. The resulting PLA conforms to MOSIS design rules. When originally designed, this module could be run on ISIS graphics workstations or a Y AX. Currently, there is no operating version of this tool available for use on any modern graphical workstation available at NPS. However, the individual cells can still be assembled by hand. and a custom layout vice a generated PLA was created for this device In the present tool, the step-up function generator modules are designed to produce output currents in the range of 150uA to 180uA. Likewise, the step-down function generators produce output currents of approximately 240uA. However, these outputs only function as input to column generators. which have a switching threshold of approximately 20uA. Thus, internally, the switching currents produced by a device implemented using these cells tend to consume more power than necessary Column generators must produce output currents that are very nearly the ideal logic values, or small errors will tend to compound quickly as terms are connected for the wired sum function. Above the switching current levels of the threshold detectors in the step-up and step down generators should ideally "split" the ideal logic values for maximum effectiveness against introduced errors. the original pla generator tool suffered from both inaccuracies in the output generator as well as at the inputs to the threshold detectors. For example, if the outputs from two column generators are wired together, and each is designed to produce a logic 1, the wired sum would be approximately 11O µA, a logic 2. However, the step-up function generator reports detection of a logic 3 input beginning at 110uA. Thus, if this wired sum was to be used as an input to another term which included the Step-up 3 function, an error would occur. Similar examples can be contrived for the step down function cells. Using new MOSIS design rules, minimum wire width is reduced from 4µm to 2 µm with a λ of 1.0µm. This allows more precise control of threshold detector values and column output generator current levels

4 3 Improved Logic Values and Switching Thresholds

In order to reduce power requirements for this design and improve noise margin performance. The logic value thresholds and the ideal current values produced by the step up and step-down generators were redesigned as follows:

Table 3: New Logic and Threshold Current Values

	Original HAMLET Design Values:			
Logic Values	**Step Down Generator**	**Ideal Current**	**Current Generator**	**Step Up Generator**
0	0µA	0µA	*	10µA
1	20µA	50µA	58µA	60µA
2	80µA	100µA	100µA	110µA
3	130µA	150µA	136µA	not defined
	New Design Values:			
0	0µA	0µA	*	20µA
1	20µA	40µA	40µA	60µA
2	60µA	80µA	80µA	100µA
3	100µA	120µA	120µA	150µA

A substantial power savings was alsorea1ized by reducing the current output from the step up and step down cells. The column output generators require much less current for switching purposes than in the original HAMLET design. Table 4 summarizes the redesign of the step up/down generator output current levels.

Table 4: New Step up and Step Down Generator Output Current Design

Output Currents From Step Up/Down Generators:		
	Step Up Generator	**Step Down Generator**
Original Cells	180µA	240µA
New Cell Design	60µA	70µA

4.4 Simulation of New Cells

The individual circuits were implemented using MAGIC and then extracted to SPICE for simulation and analysis. Because of the nature of multi-valued logic, the normal definition of noise margin does not apply. For this circuit, the noise margin can be defined as the: difference between the output logic level and the input switching thresholds of the next gate. The optimum noise margin can be achieved only by centring the output logic value between its associated switching thresholds. These nominal Current values have been achieved within 2µA. The timing delays and power consumption of the various components are detailed below.

Table 5: Timing and Power Simulation or Cells

	Step Up Generator	**Step Down Generator**	**Column Output Generator**
T_r(ns)	4.19	1.43	1.23
T_f(ns)	2.04	3.12	1.51
T_{PLH}(ns)	11.48	4.29	2.16
T_{PHL}(ns)	2.74	9.61	5.69
P_{STATIC}(mW)	1.78(H)/ 0.0L	1.07	0.42(H)/ 0.81(L)
$P_{LH(peak)}$(mW)	1.78	1.34	0.87
$P_{HL(peak)}$(mW)	1.78	2.25	1.60

5. Design and Simulations

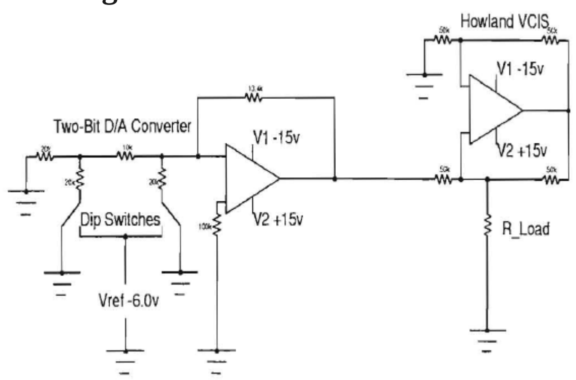


Figure 3: Testbench Input Circuitry

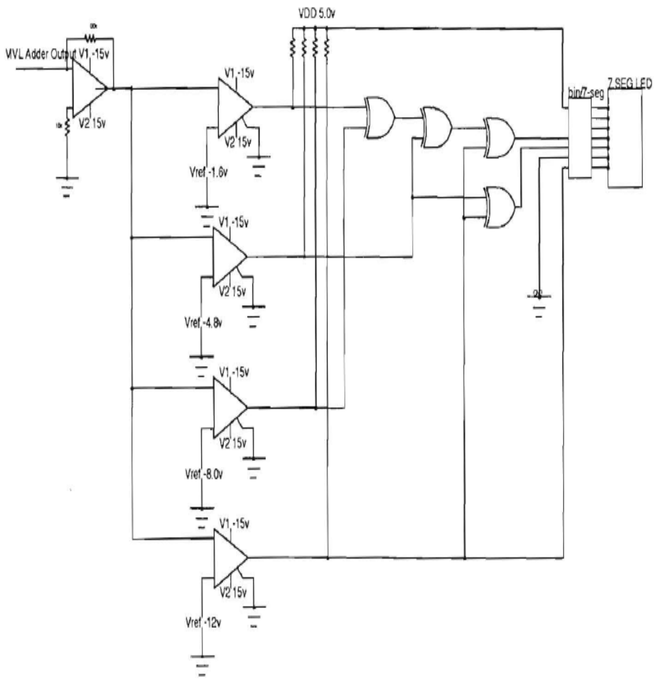


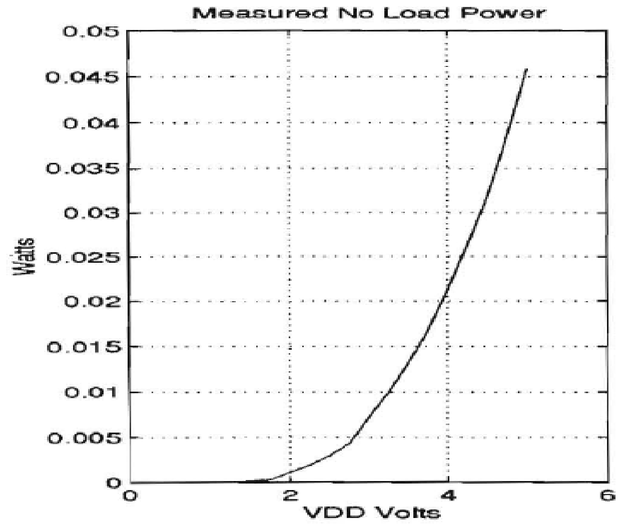
Figure 4: Testbench Output Circuitry

6. Summary of Test Results

6.1 Static Power Tests

Table 6: Component Static Power

MVL_adder Device 3		
	Design No Load	Measured No Load
Sum (right tower)	2.93mA	3.12mA
Sum (left tower)	2.88mA	3.02mA
Carry out tower	2.95mA	3.23mA
Current mirror	0	0.0mA
Pad ring	0	0.0mA



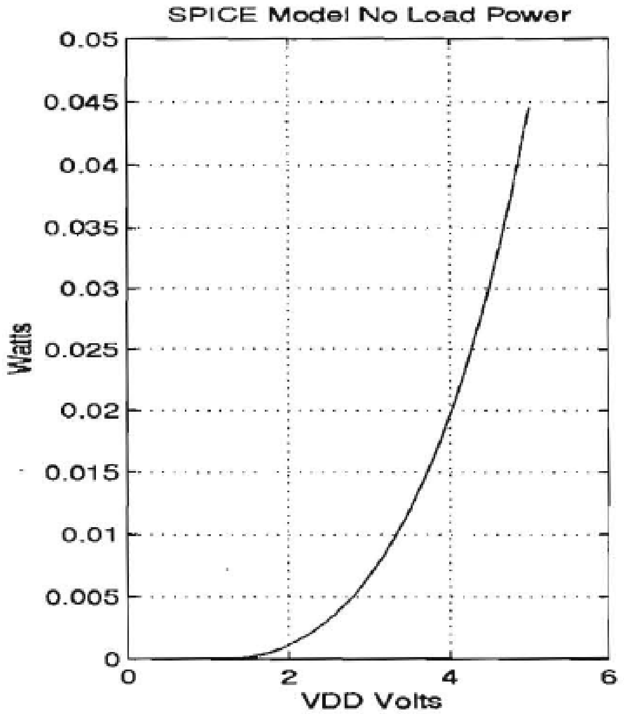


Figure 5: Measured and SPICE Simulation of No Load Static Power Consumption

Table 7: Full Power Measurement

	MVL_adder Fab ID: N46EFF1		Spice Model (VDD set 5.0v)	
	Measured Current	Calculated Power	VDD Current	VDD Power
Device 1	70.5mA	352.5mW	66mA	330mW
Device 2	69.3mA	346.5mW		
Device 3	70.2mA	351.0mW		
Device 4	69.3mA	346.5mW		

6.2 Functional Testing

Table 8: Functional Test for Device 1

	Sum Output		Carry Output	
[Xin, Yin, Cin]	design (mA)	measured	design (mA)	measured
[1,1,0]	80	82.2	0	0
[2,1,0]	120	119.3	0	0
[1,3,0]	0	0	40	41.3
[2,0,1]	120	119.7	0	0
[2,1,2]	40	41.2	40	40.3
[3,0,1]	0	0	40	40.9
[3,2,1]	80	80.9	40	40.0
[0,3,2]	40	40.3	40	40.3
[3,3,2]	0	0	80	79.2
[0,2,2]	0	0	40	40.2

6.3 Transient Analysis

Table 9: Propagation Delay

	Sum 0->3->0		Carry 0->1->0	
	measured	SPICE	measured	SPICE
t_r	280nS	60nS	223nS	10nS
t_f	254nS	110nS	215nS	10nS
t_{dr}	135nS	90nS	170nS	120nS
t_{df}	120nS	55nS	73nS	40nS

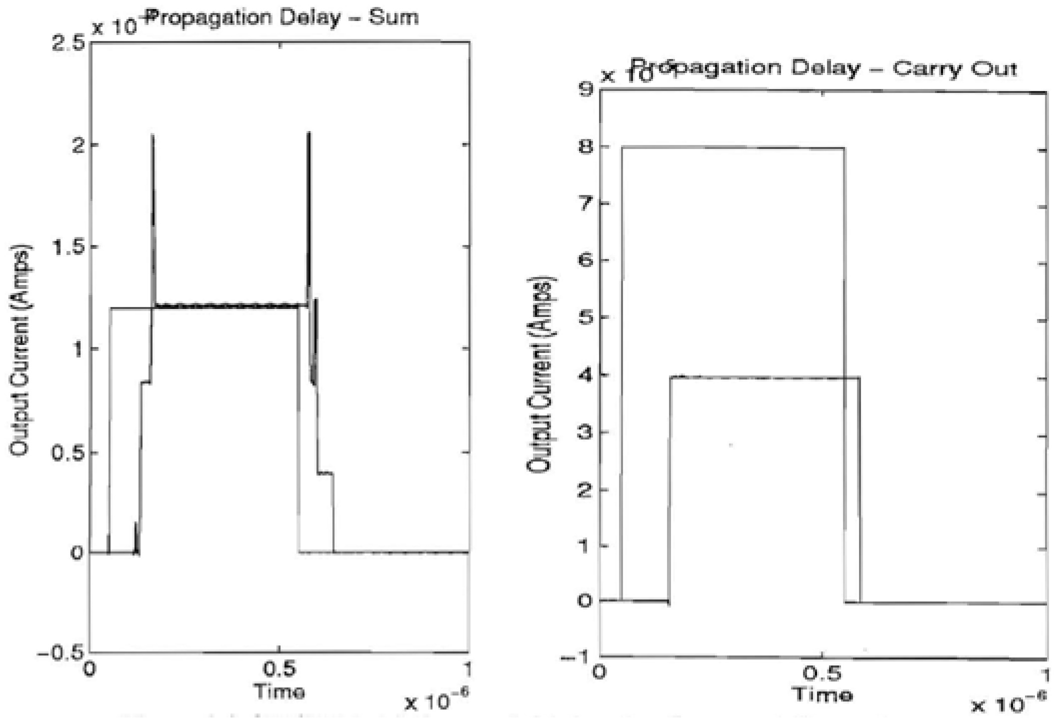


Figure 6: SPICE Model Propagation Delay for Sum and Carry Out

7. Conclusion

Steady-state functional operation conformed very closely to design and simulation Output currents were on average within I per cent of ideal operation for Vdd set to 5.Ov. This is important due to the fact that these devices are designed to operate in both parallel (carry save) and serial (ripple) adder configurations. Static power consumption for no load, full load, and peak power were very close to design values.

The timing measurements were difficult to obtain. The output currents were converted to voltage signals across a l Kohm resistor, inherently increasing propagation delays, especially rise/fall times. Measured propagation delays fell between a low of 2 and high of 20 times larger than the simulated values. In this case, the measured values are open to a certain degree of speculation for accuracy. Attempts to use smaller resistances failed to produce a voltage signal strong enough to be distinguishable from background noise. With such small measurable signals, the inherent capacitance in the testing boards and connections proved to be significant.

8. Future Research

8.1. Charged-Coupled Device (CCD) Logics

A programmable logic array implementation using CCDs is an appropriate evolutionary step for the HAMLET project. CCDs have been found to be useful in the design of memory units. Hitachi has implemented a 16 valued memory. Although multiple valued logic CCD is slower than CMOS, it is much denser. The use of MVL CCDs can increase storage capacity significantly, perhaps replacing the disk[6]

8.2. Resonant-Tunnelling Diodes (R TD) Logics

Quantum resonant tunnelling devices offer the highest speed performance for multi valued logic implementation to date. At present RIDs exist primarily as discrete devices, hence, RTD VLSI implementation and modelling is in the future. RIDs will produce extremely simple and high speed NO and D/A converters which are also a significant part of the MVL VLSI implementation problem

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