Area Efficient Architecture for Convolution Using Vedic Mathematics

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Abstract: ***Convolution is a formal mathematical operation, just as multiplication, addition, and integration. Addition takes two numbers and produces a third number, while convolution takes two signals and produces a third signal. Convolution is used in the mathematics of many fields, such as probability and statistics. In linear systems, convolution is used to describe the relationship between three signals of interest: the input signal, the impulse response, and the output signal. Vedic mathematics is used since it reduces time, increases speed and is easy to implement. It helps to solve problem 10-15 times faster. It covers explanation of several mathematical terms such as algebra, arithmetic, geometry etc. This paper presents a direct method of reducing convolution processing time using hardware computing and implementations of discrete linear convolution of two finite length sequences (NXN) The purpose of this research is to prove the feasibility of an application specific integrated circuit (ASIC) that performs a convolution on an acquired image in real time. The proposed implementation uses a modified hierarchical design approach, which efficiently and accurately speeds up computation; reduces power, hardware resources, and area significantly. The efficiency of the proposed convolution circuit is tested by embedding it in a top level FPGA .It also provides the necessary modularity, expandability, and regularity to form different convolutions for any number of bits***

Keywords*:* Convolution, Vedic Mathematics, Urdhva-Triyagbhyam Sutra, Active HDL.

1. Introduction

Convolution is fundamental operation of most of the signal processing systems. It is necessity of time to speed up convolution process at very appreciable extent .Convolution [1]on digital images is important since they represent operations that are more general than the operations that can be performed on analog images[8]. Digital images can be modified (through convolution) by neighbourhood operations; these operations go beyond point wise operations, and include smoothing, sharpening, and edge detection. Convolution has many applications which have great significance in discrete signal processing. It is usually difficult to deal with analog signals. Filtering of signals is very important in order to determine which one to accept and which one to reject, and all of that is done by convolution. Here direct method of computing the discrete linear convolution [11] of finite length sequences is used. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva Triyagbhyam–sutra. Vedic method for multiplication which strikes a difference in the actual process of multiplication. Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of all types of numbers; either small or large. Multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier [5]. Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upaveda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upasutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic math's deals with several basic as well as complex mathematical operations. The word "Vedic" is derived from the word **"Veda"** which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc

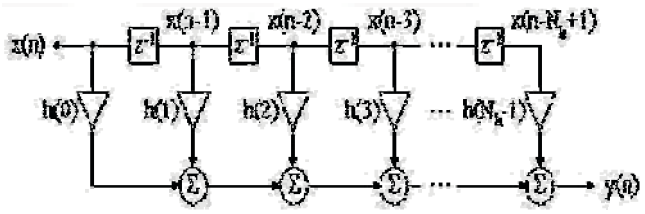
2. Convolution

It is a mathematical way of combining two signals to form a third signal [10]. For two finite discrete sequences of length N_x and N_h, the linear or a periodic convolution sum takes on a slightly different form.

$$y(n) = \sum_{k=-\infty}^{\infty} h(k)\, x(n-k)$$

Expanding Equation, the expression becomes as follows

$$y(n) = h(0)\cdot x(n) + h(1)\cdot x(n-1) + \ldots + h(N_h - 1)\, x(n - N_h + 1)$$



3. Vedic Mathematics

The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. We must be thankful to Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja to introduce Vedic Mathematics and acknowledge the work of various people regarding Vedic Mathematics. Vedic mathematics is mainly based on 16 Sutras .Vedic Sutras the word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge [4]. Vedic mathematics technique [9] is mainly based on 16 aphorisms dealing with various branches of mathematics like algebra, arithmetic, geometry etc. These Sutras along with their brief meanings are enlisted below.

1) Ekadhikena Purvena- By one more than one before
2) Nikhilam Navatshchara am Dashat-All form 9 and the from 10
3) Urdhwam Tiryagbhyam- Vertically and cross-wise
4) Paravartya Yojayet- Transpose and apply
5) Shunyam Samyasamuch haye- If the samuchchaya is same it is zero.
6) Anurupye Shunyam Anyat- If one is zero,the other is ratio
7) Sankalana Vyavakalanabh yam- By addition and by subtraction
8) Poornapoornabhyam- By the completion or non completion
9) Chalanakalanabhyam- Differential calculus
10) Yavadoonam- By the deficiency
11) Vyashtisamashtihi - Specific and general
12) Sheshani Ankena Charamena -The remainders by the last digit
13) Sopantyadayam Antyam -The ultimate and twice the penultimate
14) Ekanyunen Purvena - By one less than one
15) Gunita Samuchchayaha - Product of the sum
16) Gunaka Samuchchayaha - All the multipliers

4. Urdhva-Tiryagbhyamsutra

Urdhva-Tiryagbhyam [3] is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise. We discuss multiplication of two, three digit numbers with this method by placing the carried over digit under the first row and proceed.

Example:

```
 234
*316
----------
61724
1222---carry
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73944
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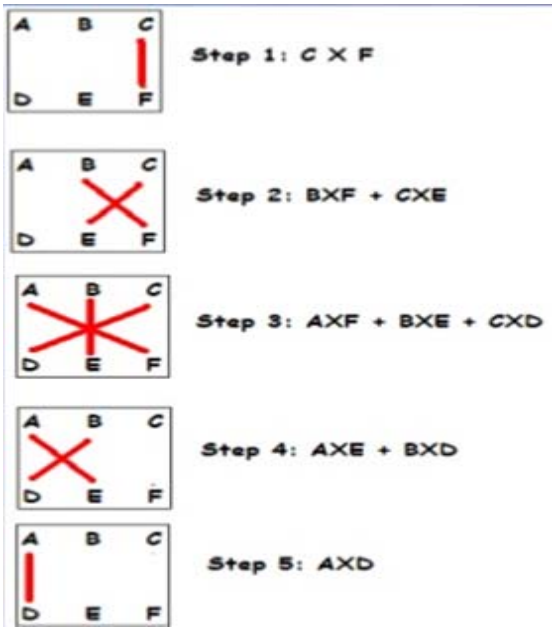
Steps:

1) 4 X 6 = 24: 2, the carried over digit is placed below the second digit.
2) (3 X 6) + (4 x 1) = 18 + 4 = 22; 2, the carried over digit is placed below third digit.
3) (2 X 6) + (3 X 1) + (4 X 3) = 12 + 3 + 12 = 27; 2, the carried over digit is placed below fourth digit.
4) (2 X 1) + (3 X 3) = 2 + 9 = 11; 1, the carried over digit is placed below fifth digit.
5) (2X3) =6
6) Respective digits are added.

Similarly for any number of digits this multiplication technique of ancient Indian Vedic mathematics can be used.



5. Proposed Methodology

- Design original convolution algorithm using conventional multiplier and adder units and verify the result then evaluate the power, and area for this design.
- Redesign the original design with reduces the number of multiplier needed using cyclic data flow, verify the result and evaluate the power, and area for this design.
- Redesign the original design with reduces the number of adder needed using cyclic dataflow, verify the result and evaluate the power, and area for this design.
- Redesign the original design with reduces the number of multiplier and adder needed using cyclic data flow, verify the result and evaluate the power, and area for this design.
- Redesign the original design with pipeline structure by incorporating latches in critical path, verify the result and evaluate the power, and area for this design.

6. Proposed Implementation Circuit

1. Type I

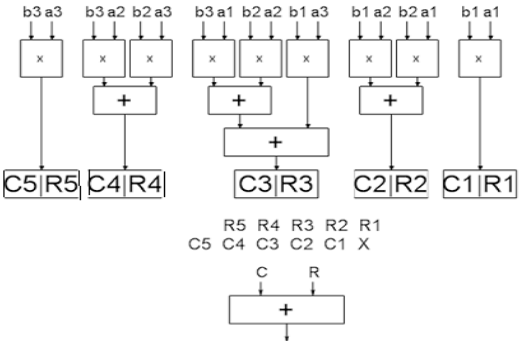


Figure 1

In this architecture 9 multipliers each of 4 bits, 4 adders of 8 bits and 9 bits are used respectively.

2. Type II

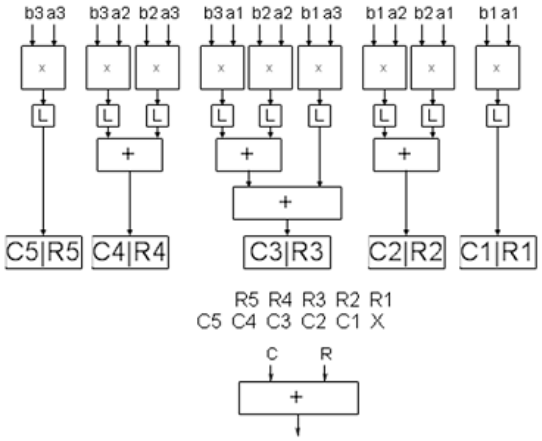


Figure 2

In this architecture pipeline approach has been implemented and latches have been used. Latches are used to stabilize the initial state

3. Type III

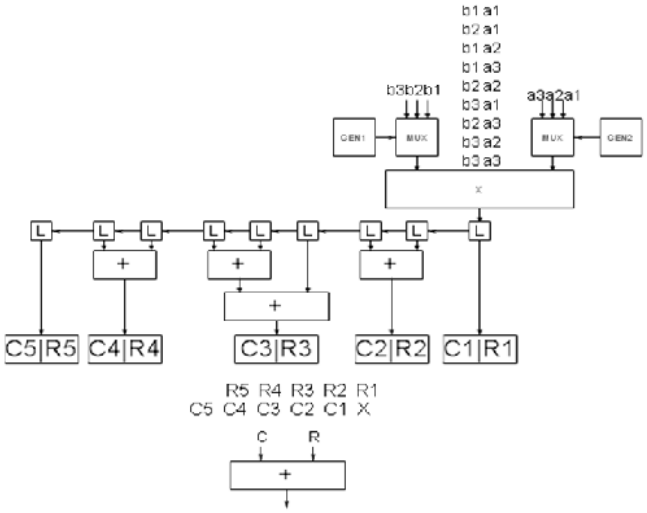
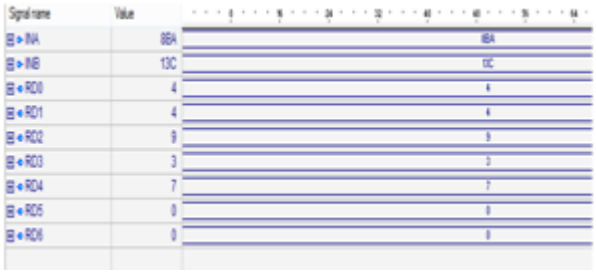


Figure 3

In this architecture 1 multiplier is used as compared to 9 multipliers in type I and II respectively.

The following is the simulation result of type1



7. Conclusion

The paper shows the efficient use of Vedic multiplication. Based on the discussion made above it is very clear that a multiplier is a very important element in any processor design and a processor spends considerable amount of time in performing multiplication and generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. An improvement in multiplication speed by using new techniques can greatly improve system performance. This project can be extended for the reconfigurable architecture

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