Baseband Processor of Multi-Purpose RFID Tag using VHDL

Anuj[1], **Ramandeep Kaur**[2]

[1]Trainee, Cetpa Infotech Pvt. Ltd, New Delhi, India

[2]VLSI Expert, Cetpa Infotech Pvt. Ltd, New Delhi, India

Abstract:-***Radio-frequency identification (RFID) is the use of a wireless non-contact system that uses radio-frequency electromagnetic fields to transfer data from a tag attached to an object, for the purposes of automatic identification and tracking. A large amount of work has been undertaken in order to optimize the performance and cost factor of readers and tags involved in the RFID system. FPGAs are considered as potential target device for implementing RFID systems. This architecture aims at the design of an FPGA implementable RFID Tag processor for the purpose of baseband signal processing. The design takes into consideration the flexibility of the entire system with the help of independent sub modules. Also, the suggested architecture has taken into consideration the creation of innovative single tag for multiple purposes which can interact with various types of readers and convey the required information to each one of them. The RFID tag has been designed in accordance to EPCglobal class1 Generation2 standard for the operation in the range of 860-906 MHz in the air interface.***

Keyword: *RFID, Baseband, tag, VHDL, AIDC*

1.Introduction

RFID is an acronym for "radio-frequency identification" and refers to a technology whereby digital data encoded in RFID tags or smart labels are captured by a reader via radio waves. RFID belongs to a group of technologies referred to as Automatic Identification and Data Capture (AIDC). AIDC methods automatically identify objects, collect data about them, and enter those data directly into computer systems with little or no human intervention.

The tag contains identification number and it is the task of the reader to retrieve it. The reader's modulator receives information from the database as to which tag is to be accessed; this information is modulated onto a continuous wave (CW) as transmitted by the antenna of the reader. Tag receives CW on its antenna, the power harvesting circuits are then activated (in case of passive tags) and incoming signal is demodulated and in accordance to that necessary information is retrieved, this information is again modulated on another continuous wave and retransmitted back to the reader. The readers demodulator receives this information and passes it onto the database after necessary processing. The database performance necessary operation on the data received and returns useful information to the user. In the design these two sub modules are integral in the implementation of Multipurpose RFID tag. The decoder helps attain selectivity in signals which are to be responded and memory element provide output for unique input. The decoder converts incoming 10 bit input into a 2 bit address which corresponds to 4 ROM addresses. The whole paper is divided into the following sections. Section I describes the architecture of the processor. Section II explains the various modules of the processor. Result has been presented in the section III.

2.Architecture

An effective adjustment to the RFID tag enables it to be used for multiple purposes. Generally, a RFID tag simple backscatters the incoming data from a reader. In this architecture we implemented a decoder and ROM component which store multiple data and enable the tag to respond to different probing signals. The probing signals from ASK modulator of the reader are demodulated by ASK demodulator at the reader. This probing signal contains the information as to which set of data is to be retrieved from the tag. The data obtained from this is passed onto the decoder that generate the corresponding ROM address for the various data stored in the ROM. Figure 1 depicts the top block of baseband processor of multipurpose RFID tag. Architecture has been shown in figure 2.

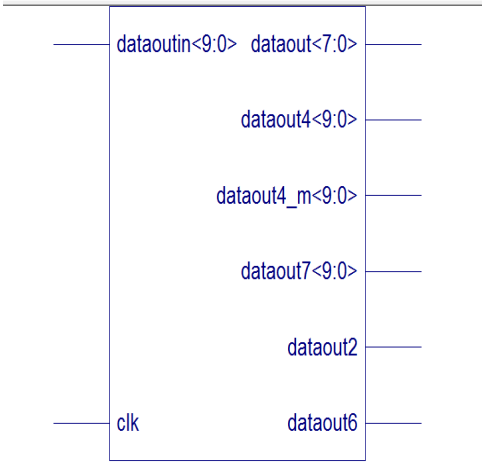

Figure 1: Top block

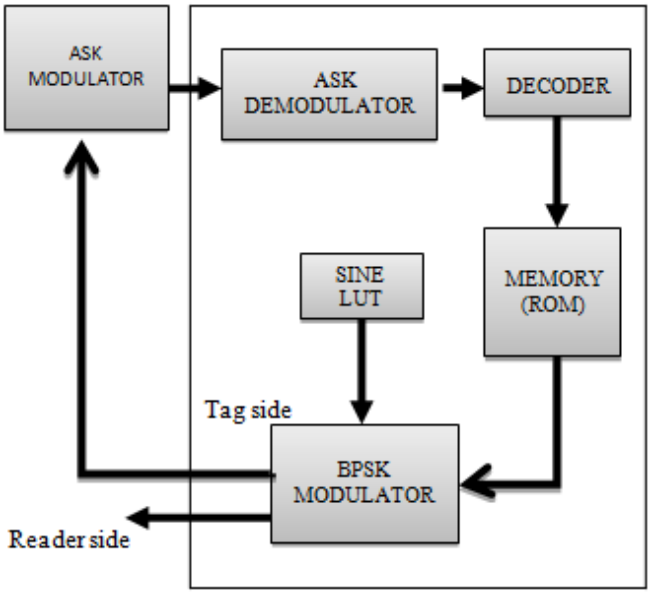

Figure 2: Multipurpose RFID Tag Architecture

3. Modules in the design of baseband processor of Multipurpose RFID Tag

3.1 ASK Modulator

Amplitude-shift keying (ASK) is a form of modulation that represents digital data as variations in the amplitude of a carrier wave. ASK uses a finite number of amplitudes, each assigned a unique pattern of binary digits. Usually, each amplitude encodes an equal number of bits. ASK Modulated waveform has been shown in the figure 3.

3.2 Algorithm

- The clock is checked for its rising edge.
- For each clock cycle two signals are prepared – one corresponding to sine wave and other corresponding to a 'zero' level.
- The incoming bit is checked for: if it is '1' then complete sine wave is sent to the output .If its zero then zero components is sent to output. Each incoming bit is spread over 30 clock cycles i.e. it is spread over whole sine wave.
- For various input bits we get the ASK modulated sine wave.

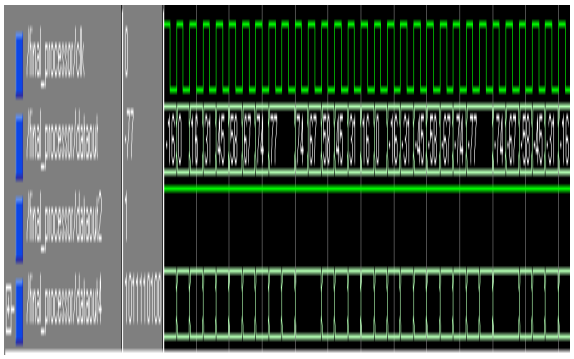

Figure 3: ASK Modulated Waveform

3.3 ASK Demodulator

The ASK demodulator is very simple to implement and is the first step that occurs when the probing signal reaches the tag. It is a simple level detector circuit

3.3.1 Algorithm

- As each individual bit has been stretched to 30 clock cycles. Hence 30 clock cycles are scanned.
- If number of non-zero are more than 15 assuming that '1' has been transmitted. Otherwise '0' is transmitted.

The value 15 has been taken because the transmitted wave might have been corrupted by noise, so that some of the original zero-level might have assumed non-zero value. If noise value is more than 15 zero values have been assigned non-zero values then there will be an error in the detection of bit. In the experimented values the demodulation gives a true representation of the transmitted signal.

3.3.2 BPSK Modulator

Tag to reader communication is done via Binary phase shift keying (BPSK). BPSK is simplest form of PSK. It uses two phases which are separated by a phase difference of 180 degree. The two different phases are used to depict the two logical levels. It is also termed as 2-PSK.This modulation is robust of all PSKs as it takes the highest level of noise or distortion to make the demodulator reach an incorrect decision. However it modulates at only 1 bit/symbol (as seen on figure) and so it is not suitable for the high data-rate applications when bandwidth is limited.

3.3.3 Algorithm

- The incoming data is considered as one bit at a time and rising edge of the clock is checked.
- Two signals are generated-one representing the sine wave from the values taken from LUT and the other representing another sine wave with phase shift of 180 degree (this is done by just negating the original sine LUT).
- If incoming bit is '1' then the sine wave is send to the output.
- If incoming bit is '0' then the inverted sine wave is send to the output i.e. one with 180 degree out of phase is sent to the output.
- Each bit is delayed so that it is spread over 30 clock cycles. This is done so that each bit is represented by a complete sine wave.
- For a continuous signal from memory, we have a complete BPSK modulated output. Here the changes in bit level (changes from '1' to '0' or from '0' to '1') are clearly observed by a change of phase.
- This information is send to antenna for further transmission to the reader.

3.4 Decoder

A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to

encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^nunique output lines.

3.5 Memory

Read-only memory (ROM) is a class of storage medium used in computers and other electronic devices. Data stored in ROM cannot be modified, or can be modified only slowly or with difficulty.

For the purpose of storing the values to be transmitted by the tag, a ROM has been used. The ROM stores 4 10 bit values which are to be transmitted in accordance with 2 bit address decoded by the decoder in accordance with the incoming probing signal. Each of the four entries in the ROM corresponding to a unique output to be given for the particular type of information requested by the reader. In our simulation we have decoded the bit stream of "1100110010" as address "11" on ROM. This value stores a 10 bit value "1100100111" which is passed onto the BPSK modulator for retransmission to the reader.

4. Result

The figure sums up the final implementation of all the blocks put together. The initial input data shown (dataout2) is that of the ASK modulator. Here a predetermined sequence "1100110010" has been used. The ASK modulated wave (dataout4) is seen to be a perfect representation of the data.Dataout8 represents the ASK demodulated data. The original data has been retrieved without any error. The data from ROM denotes the information retrieved from the memory corresponding to the data input. In this case the data retrieved is "1100100111". Finally the BPSK modulated output is shown corresponding to the retrieves data.

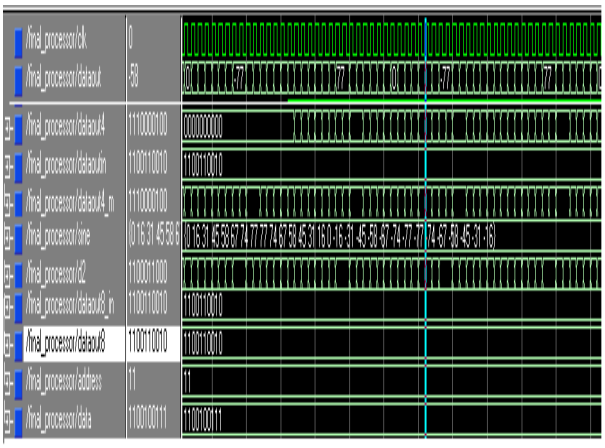

Figure 5: Processor waveform

5. Conclusion

In this paper a FPGA implementable Multipurpose RFID TAG baseband processor has been designed. The processor model was designed using Xilinx and simulation was verified using Modelsim. The reader to tag communication and its subsequent demodulation has been modeled on the same system. Hence there is no noise introduced in the system. As can be seen from the outputs, this tag processor yielded expected results. The information send by the reader was retrieved without error and desired data was taken from the memory and modulation block output was true BPSK representation of the data. In real time implementation the difference will be the presence of noise. That has been taken into account in demodulator block.

The architecture assumes modular approach for the processor. The advantage of such an implementation is that each sub module can be modified later without the use of changing the whole system. This gives scope as well as flexibility for future changes. Finally, the multipurpose nature of tag opens a range of possible applications.

6. Future Scope

In accordance with the standards used, other modulation schemes can be used for the modulation purpose and the most optimized modulation schemes in terms of bit error rate and signal power can be found out. In order to incorporate signal security, modulation techniques such as direct sequence spread spectrum can be added to the system. A power management unit can be incorporated which controls the activity of individual blocks so as to make optimal use of the power to tag. The corresponding reader can be designed to complement the architecture used in the tag.

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