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Design Low Power 10t and Comparison 16t, 14t and 11t Full Adder Using Invariant Parameter at 45nm Technology

Umashankar Dhepra[1], Rajkumar Gehlot[2]

[1]Research Scholar, LKCT Indore, India

[2]Assistant Professor. EC Department, LKCT Indore, India

Abstract: ***Power consumption has emerged as a primary design constraint for today VLSI integrated circuits (ICs). AS per reducing Technology, mostly Nanometer technology regime, leakage power has become a major component of total power. Full adder is the basic functional unit of an ALU. The power consumption of a processor is lowered by lowering the power consumption of an ALU. In this paper we introduced low power consume one-bit full adders, including the most motivating of those are analyzed and compared for speed, leakage power, and leakage current. The simulation has been carried out on a Cadence environment virtuoso tool using a 0.45-µm technology***

Keywords: VLSI, CMOS, Full Adder, leakage current, process invariance and circuit invariance

1.Introduction

In VLSI such as video processing and microprocessors, digital signal processing, and microprocessors, extensively use arithmetic operation. Addition, subtraction, multiplication, and accumulate are examples of the most commonly used operation. In this paper we present a novel 1-bit full-adder cell which offers faster operation, and consumes less power than standard implementation of the full –adder cell.

The one-bit full adder has a three-input two-output building block. The inputs are the two bits to be summed, A and, B and the carry bit Ci, which derives from the calculations of the last stages digit. The outputs are the result of the sum operation S and the resulting value of the carry bit Co. More expressly the sum and carry output are given by

$$S = A \oplus B \oplus Ci = A\overline{BCi} + \bar{A}B\bar{C}i + \overline{AB}Ci \ldots.1$$

$$Co = AB + (A + B)Ci \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 2$$

From (2) it is evident that if A=B the carry output is equal to their value. If A≠ B we have Co = Ci (the full adder is said to be in propagate mode), and hence, the full adder has to stay for the computation of Co.

2.Power Consumption in CMOS VLSI Circuits

There are three main components of power consumption in digital CMOS VLSI circuits

1) Switching power: consumed in charging and discharging of the circuit capacitances during transistor switching.
2) Short-circuit power: consumed due to short-circuit current flowing from power supply to ground during transistor switching
3) tatic power: consumed due to static and leakage currents flowing while the circuit in a stable state.
4) The power consumption for CMOS circuit is given by the following equations:

$$P_{AVG} = P_{DYNAMIC} + P_{LEAK} + P_{SHORT\text{-}CIRCUIT}$$
$$= CLV_{DD}V_{FCLK} + I_{LEAK}V_{DD} + I_{SC}V_{DD}$$

3.The 1-Bit Full Adder Different Topologies

(A) 16T 1 Bit Full Adder
(B) 14T 1 Bit Full Adder
(C) 11T 1 Bit Full Adder
(D) 10T 1 Bit Full Adder

(A) 16T 1 Bit Full Adder CIRCUIT

In this section single bit 16T full adder circuit is designed by using 16 CMOS transistor logic for improve the performance of adder in terms of power and leakage. It is the essential element of full adder cell and it generates the basic addition operation of adder cell. 16T Adder Shown in fig1 and output waveform is shown in fig 2.

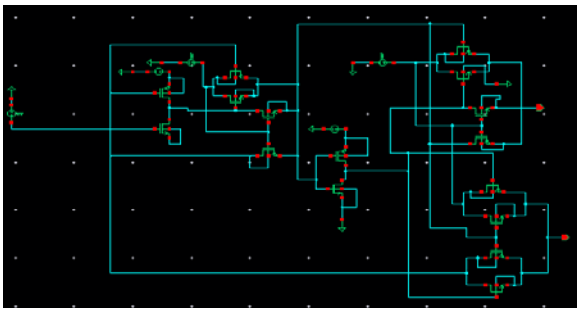

Figure 1: Full Adder using 16Transistor

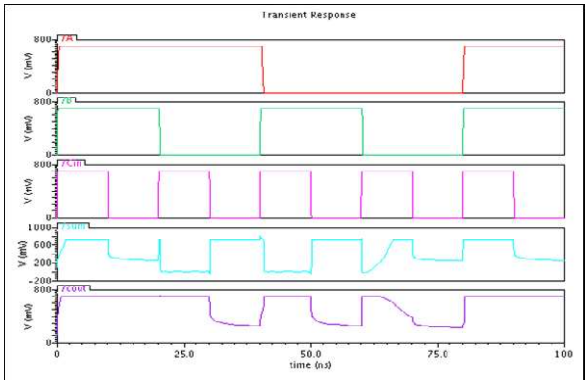

Figure 2: Output Wave form of 16T Adder

(B) 14T 1 Bit Full Adder CIRCUIT

In this section one bit 14T full adder circuit is designed by using Pass transistor logic for improve the performance of reduced power and leakage. It is the essential element of full adder cell for the basic operation of adder cell. The 14T adder shown in fig 3 output waveform is shown in fig 4

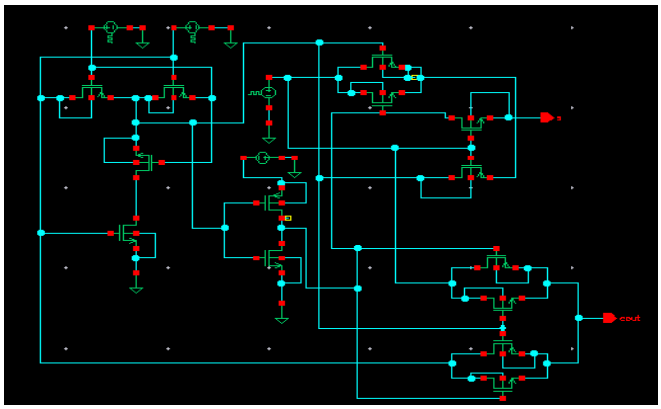

Figure 3: Full Adder using 14Transistor

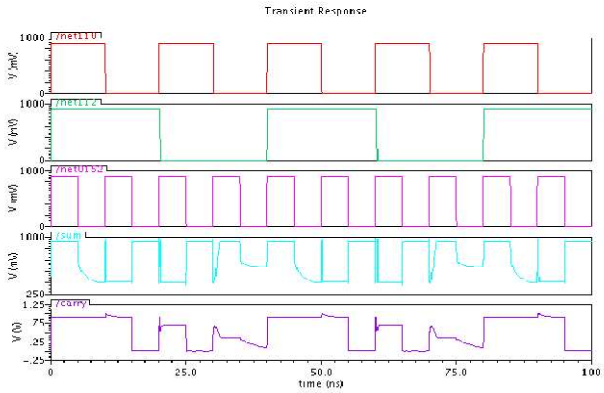

Figure 4: Output Waveform of 14T Adder

(C) 11T 1 Bit Full Adder CIRCUIT

In this section one bit 11T small size full adder circuit is designed by using CMOS transistor logic for reduced power consumption. Fig. 5 11T full adder circuit is the essential element of full adder cell operation of basic addition of adder cell. Output waveform of 11T full adder is shown in fig 5.

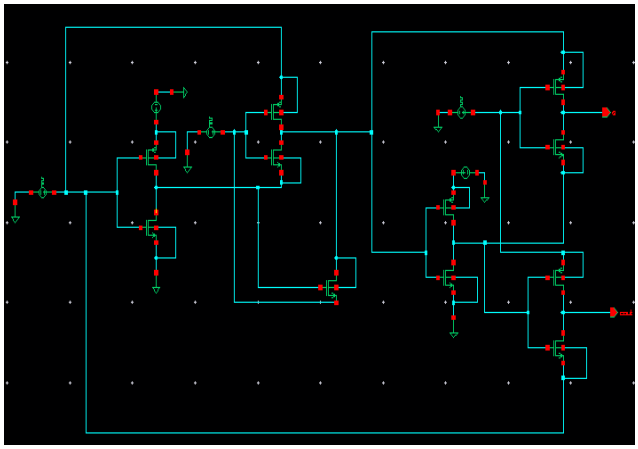

Figure 5: Full Adder using 11Transistor

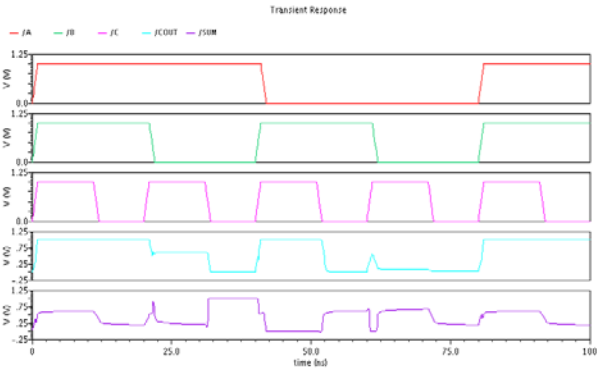

Figure 6: Output waveform of 11T Adder

(D) 10T 1 Bit Full Adder CIRCUIT

In this section one bit 10T smallest size lowest power consume full adder circuit is designed. Fig. 7 shows the 10T full adder circuit. It is the essential element of full adder cell and it generates the basic addition operation of adder cell. Output waveform of 10T full adder is shown in fig 8.

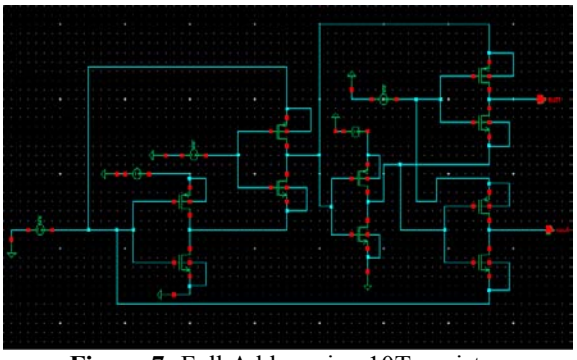

Figure 7: Full Adder using 10Transistor

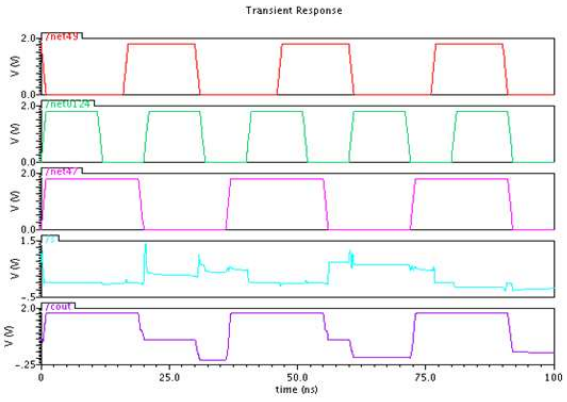

Figure 8: Output waveform of 10T Adder

4.The Proposed 10T Full Adder

The circuit of 10T Adder is a one-bit full adder cell is made of five CMOS inverters that are connected as shown in fig1. Input A is directly connected to inverter first while input B is connected second and third inverter. Second inverter PMOS drain and third inverter NMOS drain are connected first inverter output while second inverter NMOS drain and third inverter drain are connected directly input A. Second inverter output is connected fourth inverter input and input Ci is given in inverter fifth. There is interesting, the power supply VDD connected first inverter only. All transistors have minimum length (LMIN =45nm according to used Technology), while their widths are typically propose parameters.

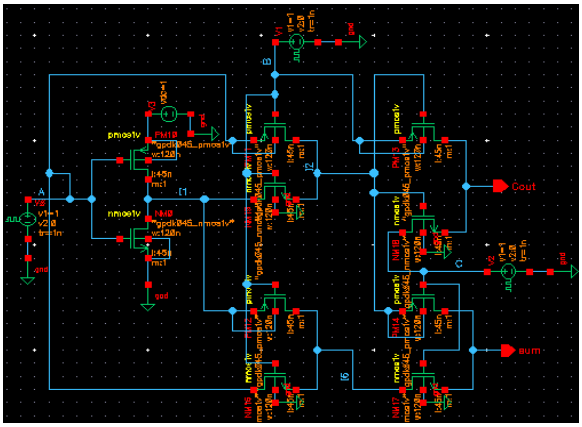

Figure 9: Proposed Ten Transistor Adder cell

Based on CMOS 0.45-nm process technology, the proposed full adder is proven to have the minimum power consumption and less power-delay product by Cadence simulation comparing with other prior literature, the characteristics of the novel hybrid full adder shows that the design has the best power-delay product for carry out signal. Output waveform with leakage current is shown in fig 10

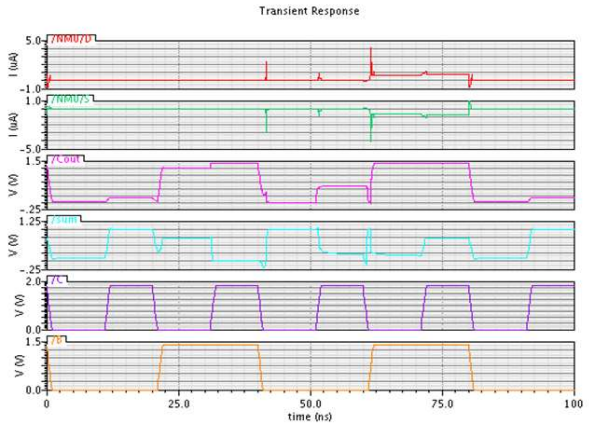

Figure 10: Leakage current graph of proposed 10T Adder

5.Leakage Reductions By Variance

a) Reverse Biasing

The body effect in CMOS transistors, a smaller width of the depletion layer leads to lower VT. The reverse biasing of CMOS transistor increases VT while on forward biasing of the COMS transistor VT decreases.

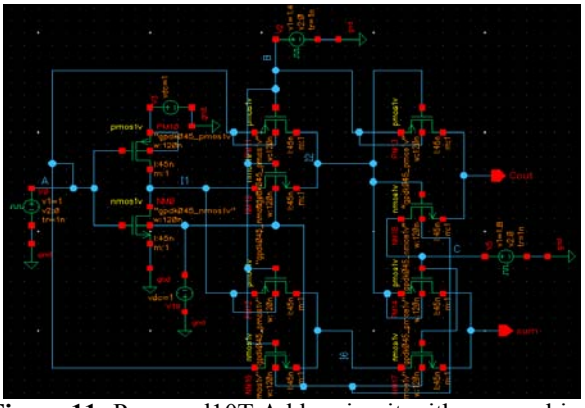

Figure 11: Propesed10T Adder circuit with reverse bias

Therefore the current in the sub threshold region can be partially decreased by reverse biasing. Equation (5) quantifies the back-gate bias parameter as function of the oxide capacitance and substrate doping level.

$$\gamma = \frac{t_{ox} \cdot \sqrt{2N_{SUB} q \epsilon_{Si}}}{\epsilon_{ox}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5$$

Where t_{ox} is gate oxide thickness, N_{SUB} is substrate doping level q is unity electron charge ϵ_{ox} is gate oxide permittivity and ϵ_{Si} is Silicon permittivity.

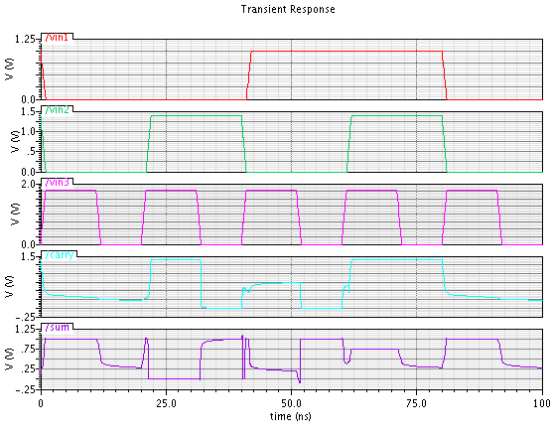

Figure 12: Leakage current with reverse bias

b) Multiple thresholds V_{TH}

The threshold voltage of the CMOS is equal to the sum of the flat band voltage, twice the bulk potential and the voltage across the oxide due to the depletion layer charge. And also in CMOS threshold voltage increases with increased doping of the channel but decreases with applied bias.

$$V_T = V_{FB} + 2\varphi_F + \frac{\sqrt{2\,\epsilon_q\, qN_a(2\varphi_F + V_{SB})}}{C_{OX}}$$

Where the flat band voltage, V_{FB} is given by

$$V_{FB} = \varphi_{FB} - \frac{Q_F}{C_{OX}} - \frac{1}{C_{OX}} \int_0^{t_{OX}} \frac{x}{x_{OX}}\, \rho_{OX}(x)dx$$

With

$$\varphi_{MS} = \varphi_M - \varphi_S = \varphi_M - (x + \frac{E_g}{2q} + \varphi_F)$$

And

$$\varphi_F = V_t \ln \frac{N_a}{n_i}, p - substrate$$

And the similar for pMOS

$$\varphi_F = V_t \ln \frac{N_d}{n_i}, n - substrate$$

The threshold voltage of CMOS is dependence on the doping density is illustrated with for both n-type and p-type MOSFETs with an aluminum gate metal.

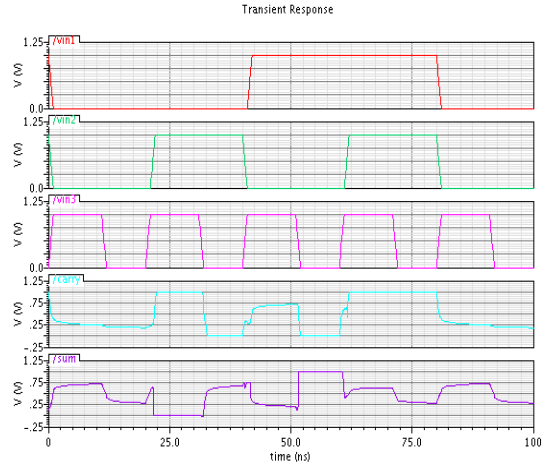

Figure 13: Transient Response of multiple doping

6.Result

We use cadence tool for simulation on in different-different technique and circuit parameter in 10T Adder cell and result that the 10T Adder is the most prominent low power consumption cell. The leakage power can be reduced by using various techniques. We have found that V_{TH} is the most appropriate parameter for leakage power and current.

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8.Future Scope

Low power is the demand of modern age And this research open a way for future very low power Adder cell with low Power processor. In this field many parameters will reduced for power reducing power consumption in Adder cell. The Low power VLSI research open new technique for reduces power in the field of Processing and Adder.

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