International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Impact Factor (2012): 3.358

Voice Characterization to Estimate the Closeness of The Unknown Voice with Reference Voice Using Spartan 6

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Abstract: ***In today's world implementation of any expert system with maximum data and networking security becomes a real necessity in academic organizations as well as in industrial communities. In this paper, an expert security system is developed using speech recognition technology. The proposed system is a chamber, which is closed by a sliding door. A smart microphone is situated in front of the door, will receive the voice samples and allows the hardware sensor to open/close the door of the system. To develop this security system, Spartan 6 FPGA is used as a hardware sensor, which is further connected with a server PC, placed inside the system for on/off control of motor. Xilinx is used to port the VHDL program in Spartan 6 FPGA. The speech recognition is performed using MAT Lab SIMULINK in server PC. This further sense the correct voice sample and sends feedback to the Spartan. Finally Spartan controls the motor of the sliding door to open/close. This VLSI designed FPGA based proposed system using Xilinx will ensure fast service compared to earlier micro-processor based VSS bio-metric switched door control. Such Spartan based system ensures the security of the system at a highest level and will also protect the system from any external undesirable threats suitably.***

Keywords: Speech Recognition Technology, Discrete Fourier Transform, spectra, secure system.

1. Introduction

Various soft-wares are used for synthesizing and analysis of hardware descriptive languages. Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs, which enables the developer to synthesize their designs, perform timing analysis, simulate a design's reaction to different stimuli and configure the target device with the programmer.

Xilinx is a supplier of programmable logic devices. It is known for inventing the Field Programmable Gate Array (FPGA) and as the first semiconductor company with a fables manufacturing model.

The Xilinx supported chips are Virtex FPGA, Spartan FPGA and XC9500 Series CPLD [1]. The Spartan FPGA comprises of Spartan – 3 (XC3S50 – XC3S1500) [2], Spartan – 3A, Spartan – 3AN, Spartan – 3A-DSP (XC3SD1800A), Spartan – 3E, Spartan – 6 (XC6SLX4 – XC6SLX75T) [3]. In this paper Spartan 6 is used as hardware where Xilinx ISE 12.4 is programmed and synthesized.

2. Proposed System

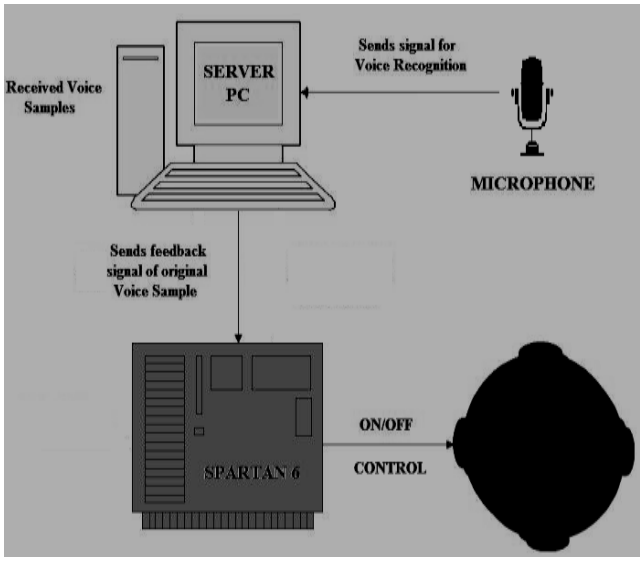

Figure 1: Proposed System

Figure 1 shows the schematic diagram of the proposed system. A microphone is situated in front a sliding door, that's opening/closing is controlled by a motor. The microphone receives the voice samples given by the external sources. These voice samples are fed to Server PC.

The input voice signal is being processed by several MAT lab SIMULINK blocks run by the server PC. In our project an Envelop Detection Method [4] is used to recognize the original voice sample for a particular word comparing with a sample voice given by any external sources. The original

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voice sample is initially stored in the server PC.
After detecting the original voice sample, the server PC sends a feedback signal to the Spartan 6 hardware device for controlling on/off the motor to open/close the sliding door of the proposed system.

3. Voice Recognition System Design

The speech processing and language technology contains lots of special concepts and technology. To understand how different speech synthesis and analysis methods work; we must have some knowledge of speech production articulator phonetics, and some other related technology [5].

In our project, a voice sample (or a particular word) which has got certain voice frequency and a definite shape for pronouncing that particular word, is processed by the Envelop Detector shown in figure 2.

Then the processor will detect the edges of that particular voice signal [6]. Finally the edges will be stored in the Server PC shown in figure 3 below. the length or size of a signal. Most often we use to insert zeros to increase the length.

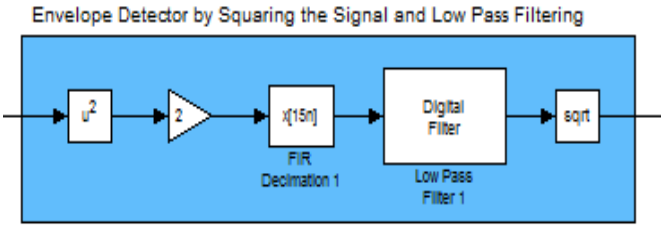

Figure 2: Envelop Detector Unit

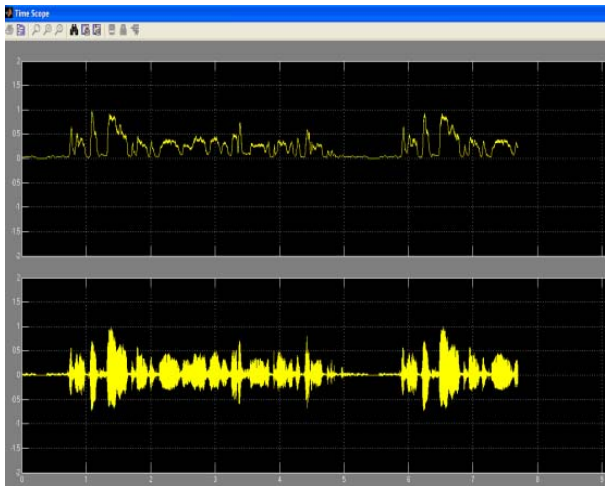

Figure 3: Edge Detected Original Signal (upper one)
Original Voice Signal (bottom one)

A. Principle of operation

The smart microphone situated at the sliding door of our closed chamber, sends the voice signal to the Envelop detector Unit (EDU). After processing the voice signal, this EDU converts the unknown voice signal to edge detected voice signal. Then this unknown signal is subtracted from the stored original voice sample signal. If these two voice signals are matched, then the output of the subtractor becomes zero. That is fed to the Embedded MAT lab function block [7]. Finally a step signal is obtained at the output of the Embedded MAT lab function block, which is further send to the input of the Spartan 6 hardware device.

MAT Lab SIMULINK is used to implement the operation of EDU [8]. The SIMULINK implementation of the voice recognition system is shown in figure 4.

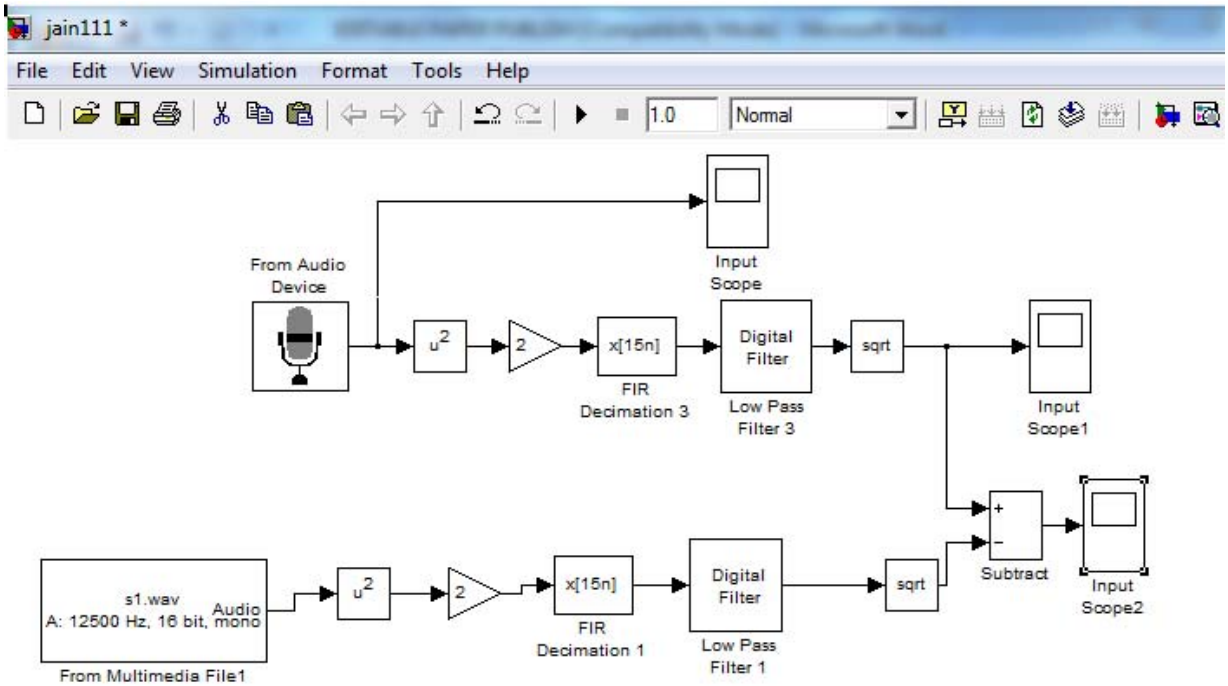

Figure 4: SIMULINK implementation of VRS design

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The voice recognition system (VRS) in our project squaring the signal and Lowpass filtering method used for detection of edges of a voice signal at the input side shown in figure 5(a) and another FIR decimation and one Low Pass Filter (LPF) are used for proper processing of the particular voice signal at the output side as shown in figure 5(b).

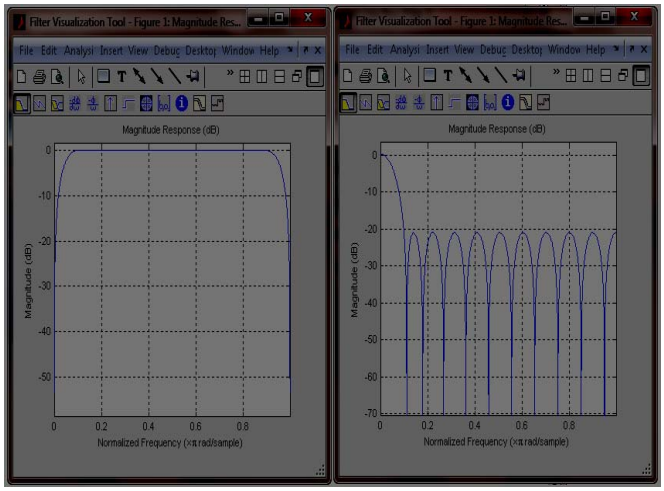

Figure 5: (a). Decimation Filter Response at input side of EDU . **(b).** Low Pass Filter Response at output side of EDU

The main strength of the developed voice recognition system is that the system provides adjustable level of security for user's convenience [9]. For example, 5% to 10% deviation i,e; 95% to 90% matches is deemed sufficient to allow normal variation of human voice when they are taken ill. This match deviation might also be allowed in case of time and attendance systems, where only medium security level is required for such expert systems. Otherwise, the security setting can be set to a higher match value when it is required.

Figure 6 shows the function block for access control. The user's voice input will be compared with the stored original sample voice and followed by a subtractor block. If the output is less than the set security level, logic 1 is produced which means that access is granted. Otherwise logic 0 is produced meaning that the access is denied [10], [11]. The resultant logic output will be transmitted through the parallel port to the Spartan 6 hardware device to perform the next task (open/close control of the sliding door) accordingly.

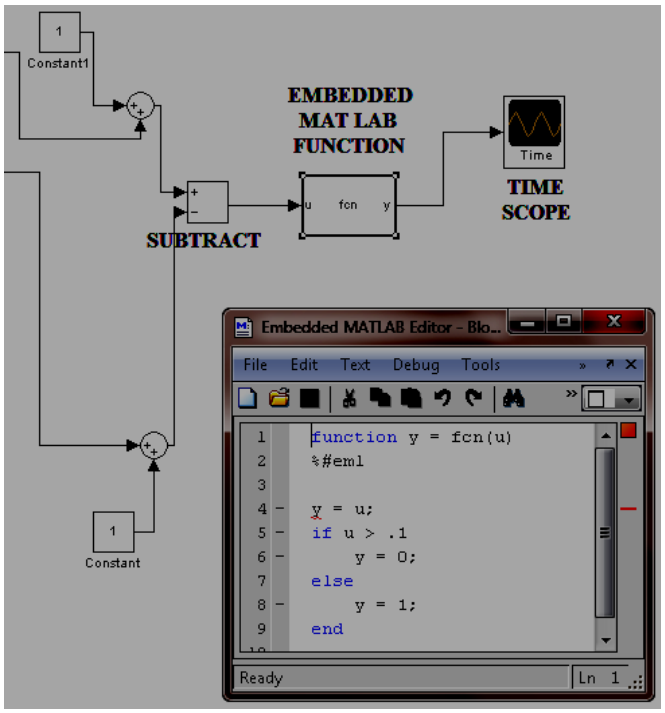

Figure 6: Function Blocks for Access Control

4. Hardware Used For XILLINX

The Atlys Spartan 6 circuit board is used for this project work [12]. This Atlys PCB is a complete ready to use digital circuit development platform based on a Xilinx Spartan 6 LX-45 FPGA. The on-board collection of high-end peripherals, including G-bit Ethernet, HDMI Video, 128 MByte DDR2 memory array, audio and USB port makes the Atlys PCB an ideal host for complete digital systems built around embedded processors like Xilinx Micro Blaze.

In this paper the Xilinx ISE 12.4 is used as software and the Atlys Spartan 6 is used as hardware device. This Xilinx ISE 12.4 is programmed and simulated successfully. Then the Xilinx program is synthesized and verified. Finally this Xilinx ISE coding is implemented on the Atlys Spartan 6 FPGA kit.

5. Speed Control of Motor Using Spartan 6

A control system is compared of two sub-systems, a plant (DC Motor) and a controller (Digital PID) [13]. The plant is an entity controlled by the controller. The controller can be either analog or digital. Basically the digital PID controller has been implemented earlier using microprocessors or microcontrollers [14]. But due to instruction time delay, in this project a FPGA based digital PID controller is used. It improves the speed of operation much more than the earlier ones which is definitely advantageous for us.

A. Principle of operation

The following block diagram shown in figure 7 describes the flow of operation of the Digital Control system.

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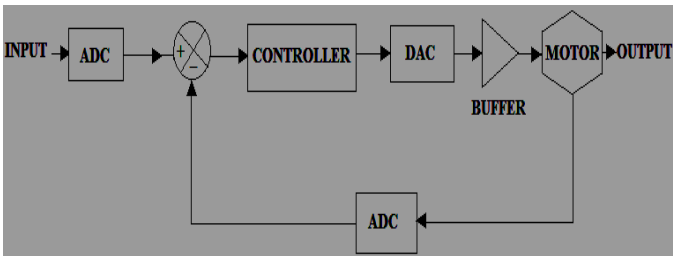

Figure 7: Block diagram of a Digital Control System

The analog input voltage is fed to an analog to digital converter. The output of the ADC sends the corresponding digital signal to the Digital PID controller for further processing. The processed signal is finally fed to the DC motor, which helps to drive the motor.

B. FPGA Implementation

The plant under test is a DC motor which is represented by the following transfer function shown in figure 8.

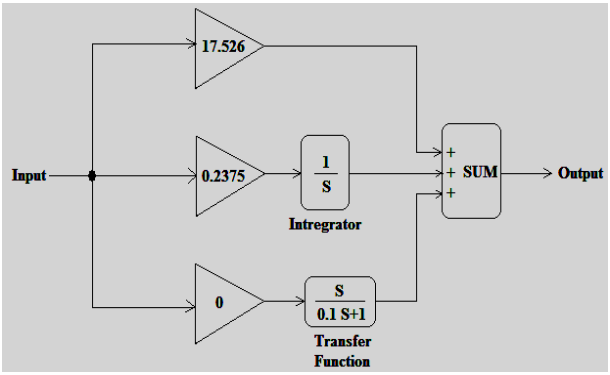

Figure 8: SIMULINK Implementation of PID controller

The speed sensor has a ratio of 0.2; the input signal was 100 mV, representing a desired output speed of 750 revolutions per minute (r.p.m.). The PID parameters for this required output speed are shown in figure 8 by using sampling frequency of 10 KHz [15]. The above PID controller will operate accordingly depending upon the transfer function. The System generator implements the design by considering the correct hardware platform and also takes care of the synchronization and interfacing problems. The flow chart of FPGA implementation is shown in figure 9.

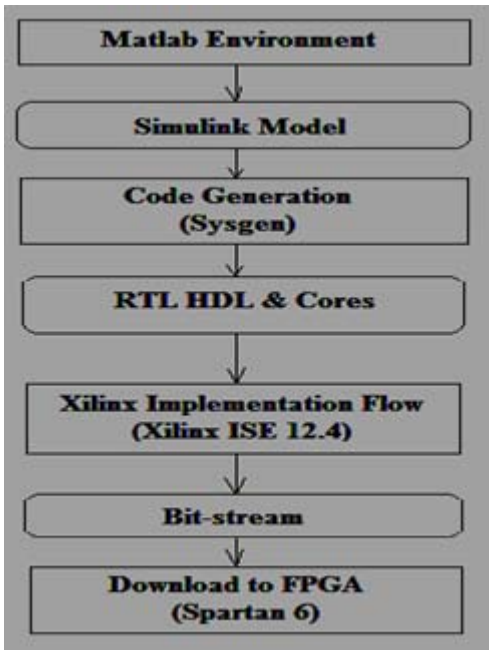

Figure 9: Flow chart of FPGA Implementation

The system generator is Xilinx tool box available with MAT Lab [16]. The blocks used for design and implementation using SysGen are shown below in figure 10.

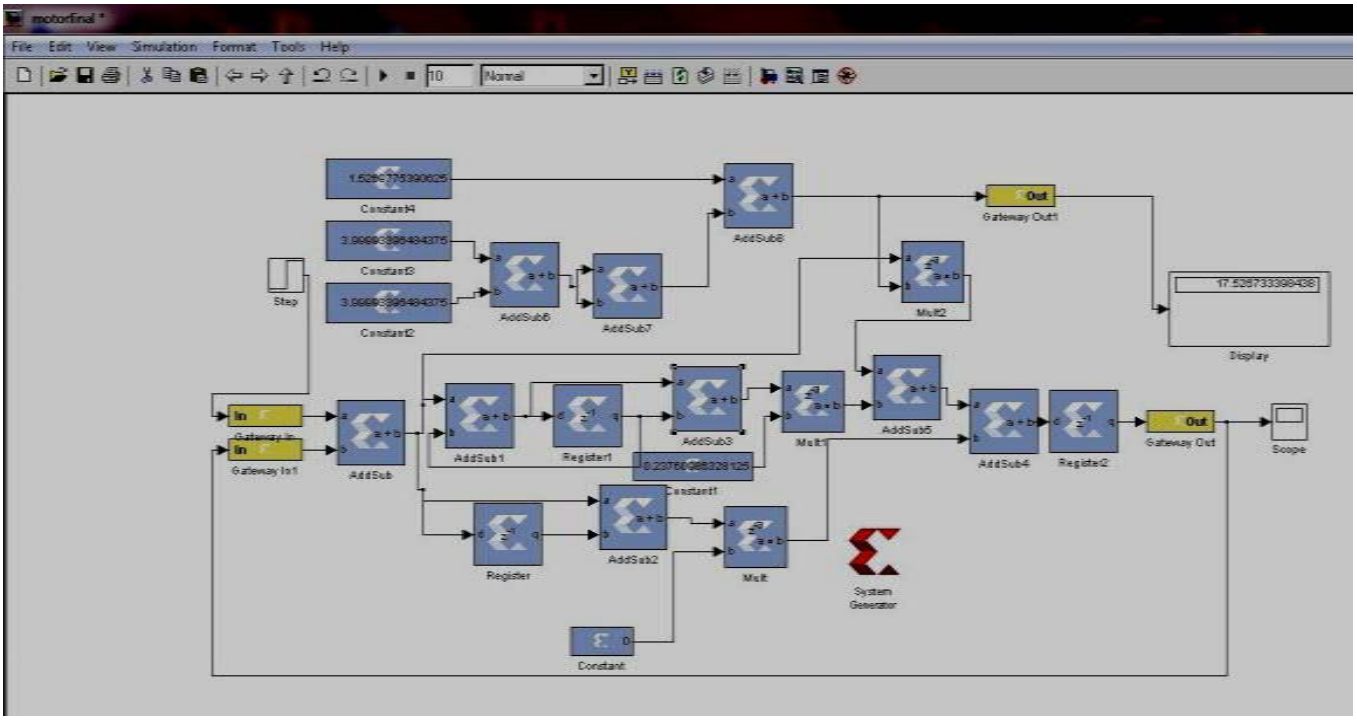

Figure 10: SysGen Implementation of PID controller

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Finally the Spartan 6 hardware device processes the input signal from server PC and sends the controlled output signal to drive the DC motor for on/off controlling of the sliding door. Practically this project is fast enough compared to micro-processor based VSS Bio-metric switch (fig. 11).

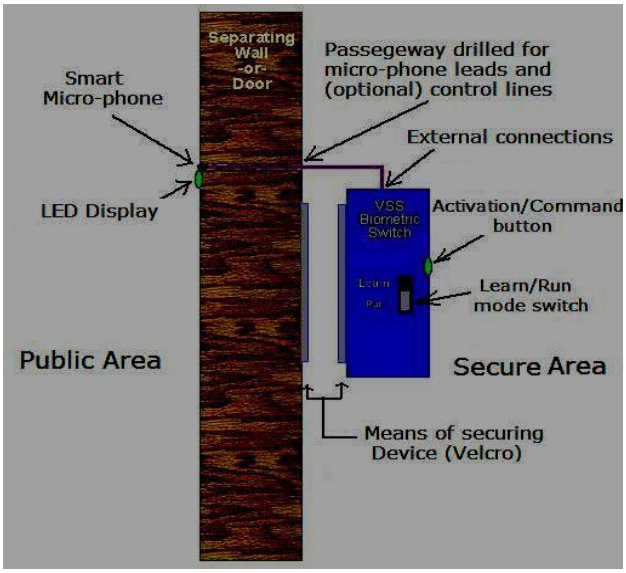

Figure 11: Micro-processor based VSS Bio-metric switch for door control

6. Conclusion

Compared with the micro-processor based door control system, our proposed smart FPGA based system provides fast response as it requires no such delays. Though our proposed system is slightly costly than the earlier one but this new bio-metric system using Spartan FPGA is much faster and more secure than the other secure (speech recognition domain) bio-metric systems. After matching the voice sample with original voice sample a step signal will be sent to the input of the Spartan 6 hardware. Finally the output of Spartan 6 helps to drive the DC motor which mainly controls the open/close of the door of the Security system.

7. Future Recommendations

Now a day's biometric technology such as finger prints [17], voice prints, iris scan [18], face detection [19], signatures or the geometry of the hand are becoming increasingly popular due to the use of unique physical traits. In voice identification technology is still slow to take off in many markets because it is not as accurate as other biometric technologies due to the tendency to have a high flash reject rate because of background noise and other variables. However with the advancement of signal processing technology better vocal synthesis, analysis and measurements using sophisticated algorithms can be taken and converted into a voice print, a unique digital representation of an individual's voice. This technology helps businesses and governments to fight identity threat and fraud, secure transactions, protect confidential information, reduce costs and enhance level of service.

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Author Profile

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