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Design and Implementation of Smart Reliable Router Switch for Dynamic NOC

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Abstract: ***In this paper we presented new router architecture, it includes an advance routing logic and error detection mechanism. So it is well suitable for the network under heavy traffic conditions .This proposed algorithm gives a better solution to avoid livelock and deadlock conditions. it will shows 100% of the error detection .In this proposed algorithm the Network on Chip (NoC) data packets are protected by using error correcting code(ECC) of hamming and switch-to-switch error detection. The designed NoC architectures are simulated and the required parameters are calculated using the tool ModelSim, which is used as a simulation and debugging tool for VHDL, verilog and mixed language designs and the tool Quartus, which is used to synthesis the network designed using VHDL Hardware description language.***

Keywords: NoC, SoC, deadlock, livelock, ECC, Dynamic NoC

1. Introduction

Now a day the trend of embedded systems has been moving toward multiprocessor systems-on-chip (MPSoCs) in order to meet the requirements of real-time applications. But the complexity of these SoCs is increasing and the communication medium is becoming a problem of the MPSoC [1], [2]. So, integrating a network-on-chip (NoC) into the SoC provides an effective. The chip employing on the NoC consists of network clients such as DSP, memory, controller, and processors. The NoC improvise the scalability of SoCs, and the power efficiency of complex SoC compared to other designs. The NoC comprises router and the interconnection allowing communication between PEs and IPs. The NoC medium features a high modularity, flexibility, and throughput. A NoC comprises routers and interconnections allowing communication between the PEs and IPs. The NoC relies on data Packet exchange. A NoC is a communication subsystem on integrated on chip. In NoC the Components just send packets, and they do not care on how the packets are routed in the network.

But the NoC is viewed as the ultimate solution to avoid problems that will arise because of the growing size of the chip. A generic NoC architecture is characterized by the number of routers, each of which is attached to processing elements in the array, the bandwidth of the communication channels between the routers, the topology of the network and the mechanism used for packet forwarding.

The topology of the network is defined through the arrangement of routers and processor on the device and the way those processors are connected together. One of the most used topology is the 2-D mesh network, because it naturally fits the tile-based architecture on the chip, and the main components which used to built this Network on Chip is router and processing element. It uses the wrapper to communicating between them and the router uses buffer, control logic and output arbiter to make the proper routing function.

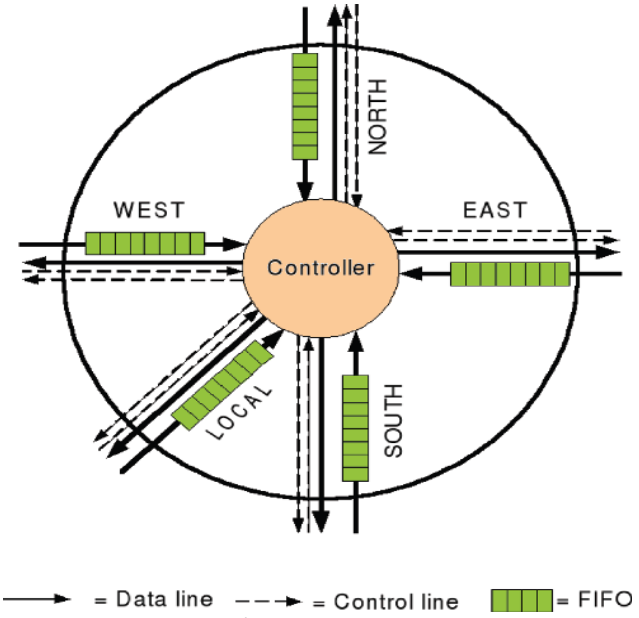

Figure 1: Router

It is includes correcting of error occurring in the transmitted data using hamming codes. The limitations is that even if the path and the transmitting data is processed correctly the architecture of the hamming code is prove to fault and it cannot be used for brust error correcting of message. To avoid both livelock and deadlock reliable router architecture is proposed by replacing under different traffic conditions [3], [4], [5].

2. Proposed Architecture

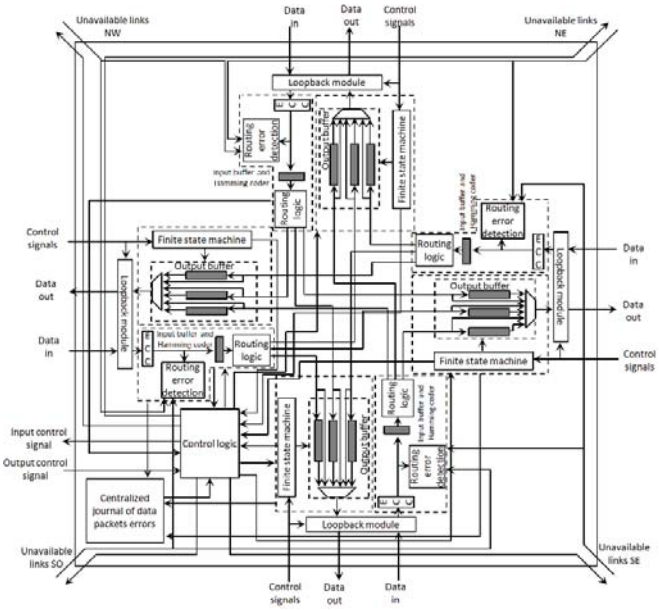

Figure 2: RKT Switch

The proposed architecture is RKT-NOC switch; it will overcome both dead and live locks. It will support to any network & supports to adaptive routing algorithm. The figure of the RKT-switch is shown in fig 2. It is suitable for a 2-d mesh NoC, having four directions (north, south, east, and west) and the PES and IPS can be connected directly to any side of a router. So, there is no specific connection port for a PE or IP. The proposed algorithm having no of blocks, they are loopback module, ECC, routing error detection, routing logic, i/o ports, i/o buffers, and control signals, it operates based on store and forward method .store and forward is a technique in which, at each node the packets are stored in memory and the routing information examined to determine which output channel to direct the packet. This is why the technique is referred to as store-and-forward (SAF). Additionally, by transferring an entire packet at a time, the latency for a packet is the number of routers through which the packet must travel multiplied by the time to transfer the packet between the routers.

A. Routing Logic

Routing is the important point to be considered, which shall act as the backbone to avoid deadlock and live lock. The routers are address in the matrix format .There were two types of logic used namely Deterministic and adaptive or both the types can be combined to be used for dynamic reconfigurable network structure

A deterministic routing algorithm provides a unique path from a source to destination. XY-routing also called dimension ordering routing is a simple deterministic routing algorithm, where messages are transmitted fully in each dimension, beginning with the lowest dimension available. In a 2-D mesh network, XY-routing first routes packets along the X-axis. Once it reaches the destination's column, the packet is then routed along the Y-axis until the destination's line. Therefore, any packet moving in the Y-direction can never return to the X-direction. This routing logic will follow a loopback module to avoid deadlock and live lock.

B. Loopback Module

The RKT switch consists of a loopback module block which is used to make a new path for the packets by looping back through another port. It is done if and only if the current router found any fault in the neighbour router to which the packet has to be sent. The circuit representation of this loopback module is given in Fig.3 which consists of buffers, multiplexer, a cross bar switch and control logic to control the operation.

In the operation of loopback module it initially checks the data request in signal from the router to which it has to send the packet if it is high and the unavailability link is low then the control logic generates control signal for multiplexer and the crossbar switch to pass the message in and out through the loopback module and activates the data request out signal. Similar to this function there were another two condition that is the data request in signal is low and the availability link is either low or high or else the availability link is low and the data request in signal is high, the control logic generates the control signal for multiplexer and the crossbar switch to loopback the signal through another port, and at the time of looping back the signal there is a chance for making a delay in receiving the data through that port to avoid this at the time of looping back the data the occ_out is activated to stop sending data to that particular port from the neighbour.

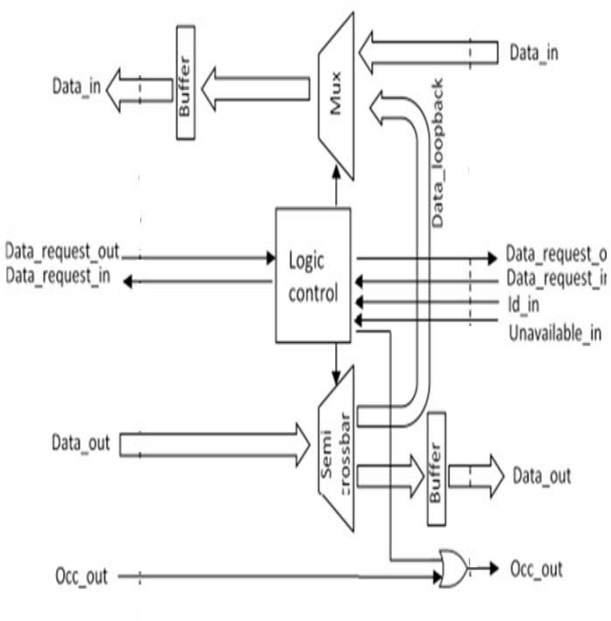

Figure 3: Loopback Module

C. Routing Error Detection

The occurrence of error is not only due to the change in the value of the message being sent it also occur due to the wrong routing path, due to the wrong routing path the live lock and deadlock occurs. Hence to avoid this particular routing error detection is added with this RKT switch. When a message is passed from one IP core to another IP

core via certain router it has to check whether it is operating correctly for that purpose a router has to check initially that the router is the current operator and weather the previous router obeys the XY algorithm, if it obeys the algorithm then the router conformed that the router has no error or else further it checks the availability of the router in the path by checking the diagonal availability indication. On checking that availability link if the router in the path is unavailable then checks weather the input for this router is for bypass operation if not it says the router has an error or else it confirmed that the router has no error.

3. Results and Performance Evaluation

A. Simulation Results and Performance Evaluations

The designed NoC architectures are simulated and the required parameters are calculated using the tool ModelSim, which is used as a simulation and debugging tool for VHDL, verilog and mixed language designs and the tool Quartus, which is used to synthesis the network designed using VHDL Hardware description language[2], [6]–[9].

In this designed reliable NoC the message takes an alternative path to reach the destination if there is any fault in the path through which it has to transmit the message, thus the message reach the destination even the router in the transmitting path is faulty. The simulation output for both non faulty networks is shown in Fig.4

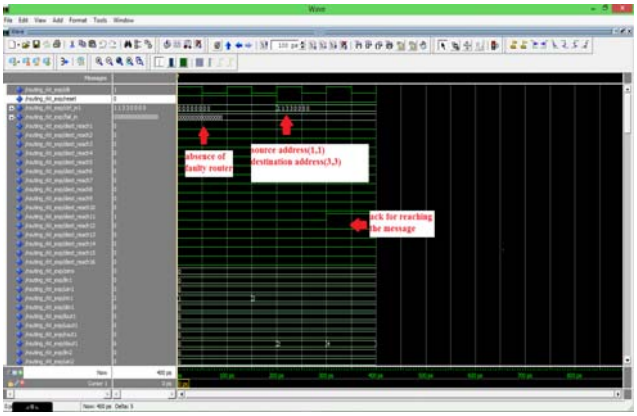

Figure 4: Simulation without any fault

The main advantage in this designed router is that the message can reach the destination even there is fault in the path through which the message travels and the simulation output for a network with faulty node is given in Figure 5.

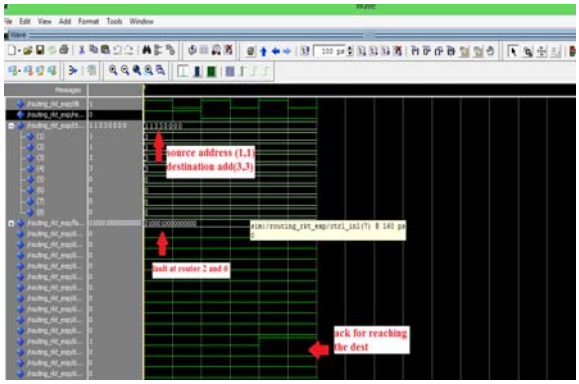

Figure 5: Simulation with faulty node

The RTL schematic for the designed RKT-NoC is given in Fig.6 which is a 4 × 4 2d mesh network.

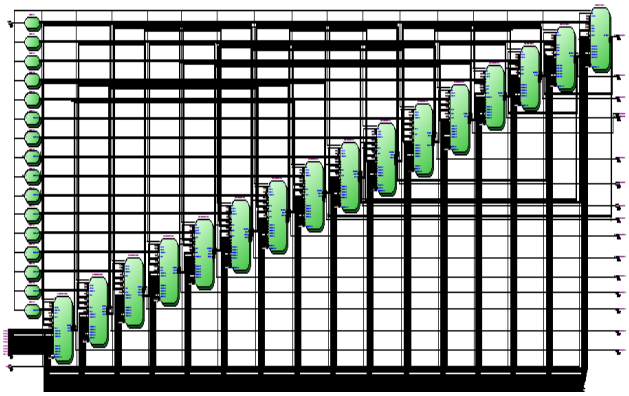

Figure 6: RTL schematic for RKT-NoC

B. Synthesis Results And Performance Evaluations

FPGA Synthesis Results:The results presented are obtained considering RKT switches configured to process data packets of four flits and able to hold two data packets in each input buffer. Table III shows the synthesis results of 4 × **4** RKT-Switch synthesis results using cyclone- II that are slices ,registers, delay(tco), FIR frequency (Mhz) and power for different sizes of data bus and FPGA technologies (Cyclone-II Quatrus FPGA).

Table I: 4 × 4 Rkt-Switch Synthesis Results Using Cyclone- II

Databus width (bits)	Slices	Registers	Delay(tco) Ns	FIR Frequency (Mhz)	Power(Mw)
4	48	16	7.159	380.08	73.67
8	59	16	7.837	380.08	74.77
16	61	16	7.963	380.08	76.01
24	61	16	7.963	380.08	76.01
32	60	16	7.658	380.08	77.05
64	60	16	7.587	380.08	78.17
128	62	16	7.773	380.08	79.30
256	65	16	8.631	380.08	80.18

It can be seen that for **4×4** the 64-b RKT-switch requires 223 registers and 959 LUTs and can operate up to 217.34 MHz on the Cyclone-II FPGA technology. We have also synthesized RKT-NoC for several sizes on the Quartus Cyclone-II technology. These results are given in Table III. The synthesis results clearly show that our architecture can be efficiently implemented in FPGA technology. It can be stated that an attractive trade-off between high speed and logic resources has been achieved.

In this paper we calculated latency, throughput. For a 2 × 2 RKT-NoC, the maximum average latency is 14 and throughput of 2 ×2, 3×3 and 4 ×4 are 2650.8, 5404.2 and 1803.7 for data bus width of 256. The maximum frequency Rate is 380.08the equations for latency and throughput are

$Latency_{RTRmin}=N_{flit}+Latency_{ECC}+3$
$Throughput_{max}=N_{IP} * n * FIR_{max} * f$

Table II: Throughput Evaluation for RKT-NoC Size of 2 × 2, 3 × 3 and 4 ×4

	RKT-NoC Size		
	2 × 2	3× 3	4 × 4
Data bus width (bits)	Throughput	Throughput	Throughput
4	42.4	101.9	34.0
8	88.7	212.8	62.1
16	172.7	370.9	122.2
24	287.5	596.2	183.3
32	361.9	881.8	224.1
64	695.6	1533.9	513.0
128	1286.5	2691.2	1001.4

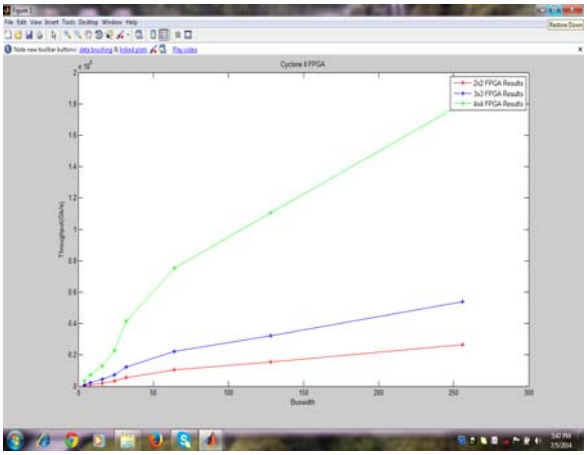

Figure 7: Throughput of one RKT-switch for different data widths

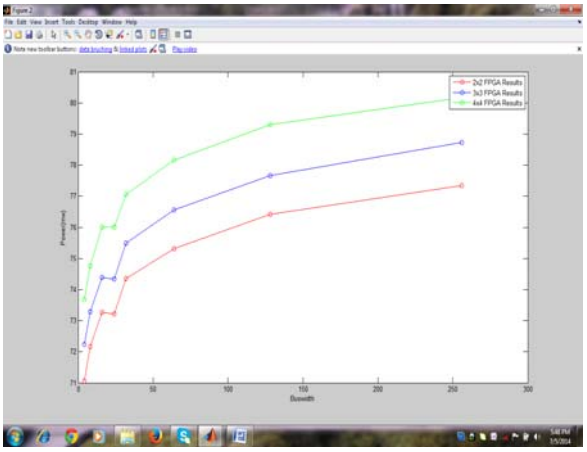

Figure 8: Power of one RKT-switch for different data widths

4. Conclusion

The RKT-NoC is highly reliable when compared with ordinary NoC due to the addition of error detection mechanism in the design and it avoids the dead lock and live lock problem. Hence it shows better performance in operation and due to the presence of error correcting code the repeated usage of the logic elements reduces and hereby it is clear that the designed RKT-NoC is more advantageous than the ordinary NoC.

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