International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Impact Factor (2012): 3.358

Dynamic Power Reduction in CMOS Logic Circuits using VID Technique

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Abstract: ***VID is a new technique for complementary metal-oxide semiconductor (CMOS) gate design that has different delays along various inputs to output paths within the gate. Here demonstrate the use of the variable input delay CMOS gates for a totally glitch-free minimum dynamic power implementations of digital circuits. We obtained a power saving of 58% over an un-optimized design. The optimized circuits had the same critical path delays as their original un-optimized versions. Since the overall delay was not allowed to increase, the glitch elimination with conventional gates required insertion of delay buffers on noncritical paths. The use of the variable input delay gates drastically reduced the required number of delay buffers.***

Keywords: Introduction, Background, Previous work with Variable Input Delay, Dynamic Power reduction, Experimental Analysis, Conclusion.

1. Introduction

The low power design has the 3main components: AREA, DELAY and POWER. All 3 components had to reduce for low power design of any circuit. In the CMOS logic circuits the power reduction is much more cause of glitches or switching activities and it can't be reduced due to switching. It can be reduced by the circuit design technique.

Whenever a logic gate changes state, power is consumed. The state change can be due to the essential logic value changes as well as due to glitches. The reasons for the glitch activity in a digital circuit are the hardware delays. There are discussed about the VID method for glitch reduction in CMOS logic circuits.

Tejaswi Raja introduced VID technique in 2004 and improved the technique with buffer insertion methods. This is used for the dynamic power reduction. There are buffers inserted in path delays which reduced the power of 50%-58%.

2. Background

There are described the background of the technique for low power design of the circuits. The VID technique reduced the glitch reduction in CMOS circuits with buffer insertion.

Delay Elements in CMOS circuits
In the CMOS logic circuits power consumed in 3 ways: Dynamic power, Short circuit power and Static power. The Dynamic power caused by the switching activities or glitches, this power can't be reduced. It reduced with the circuit design. The Short circuit power caused by the short circuit fault in the circuits and reduced simply with the power off the circuit. The Static power caused by the leakage power in the circuits, it can be reduced with different techniques. The paper focused on the reduction of Dynamic power in CMOS circuits.

There are following techniques used for the dynamic power reduction:

$$P_d = AfV^2 \quad \text{(i)}$$

a) Power reduced by the reduction of switching activity in the circuit.
b) Power reduced by the reduction of the operating frequency of the circuit.
c) Power reduced by the reduction of the supply voltage of the circuit.

There are main problem is switching activity which consume more power and it can't reduced easily. Glitch power consumption can be as much as 40%

A new technique used for dynamic power reduction in 2004. Raja et al described VID technique for glitch reduction. This technique improves the design of the circuit in terms of delay reduction. The advantage of this gate model is that glitches can be completely eliminated from the circuit without the insertion of any delay buffers, thus achieving more power saving.

3. Previous Work

There are three possible ways of implementing the variable-input -delay gate and its application to low power design. The technique for the sizing of the new gates and delay elements is also discussed in recent publications.

It is to be noted that this technique is different from input reordering techniques, because the amount of delay difference between two paths through a single gate that can be achieved by input reordering is much smaller compared to that achieved in the designs. Dynamic power consumption in circuits can be described as the product of number of transitions and average power per transition. Our technique reduces glitches in the circuit thereby reducing.

This paper studied the technique with the design conventional gates, combinational circuits. Also discussed the technique with implementation of arithmetic circuits.

4. Experimental Analysis

In this paper considered VID technique with an arithmetic circuit Full Adder. The experiment performed on Xilinx-13.1

with VHDL coding. The experimental analysis is required for the implementation of technique. There are the VHDL coding used with the Xilinx-13.1 and simulation done with the ISIM simulator.

Synthesis code first written for a Full adder circuit without using VID concept. After synthesize the code simulation done and timing report generated which provides the gate delays in the circuit and also defines the design specification for circuit. The RTL schematic and synthesis report of the circuit without using VID technique given as:

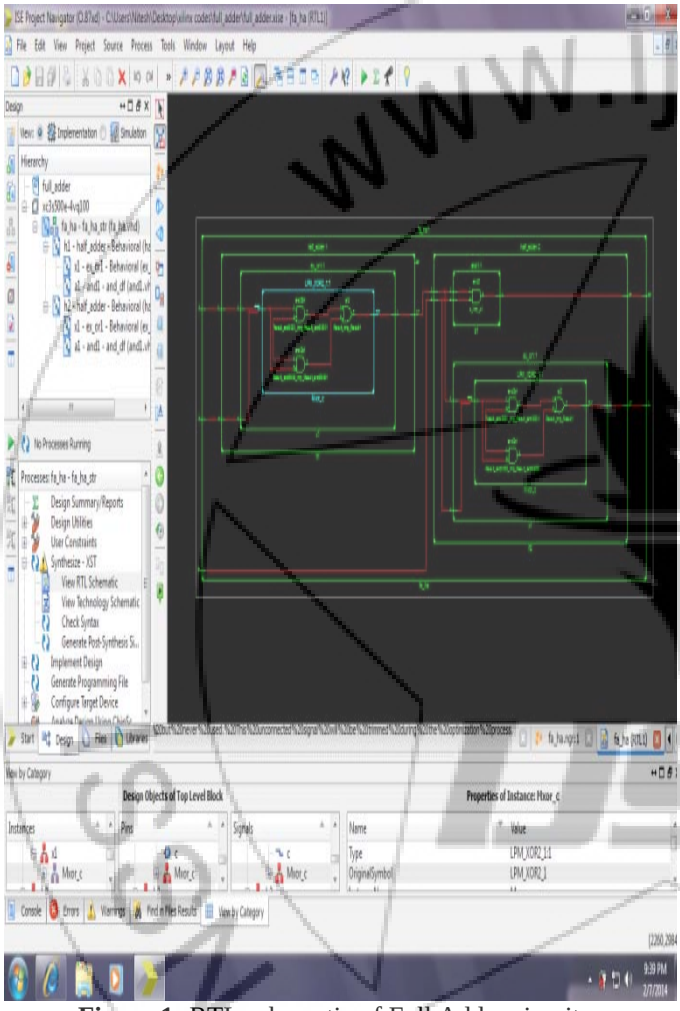

Figure 1: RTL schematic of Full Adder circuit

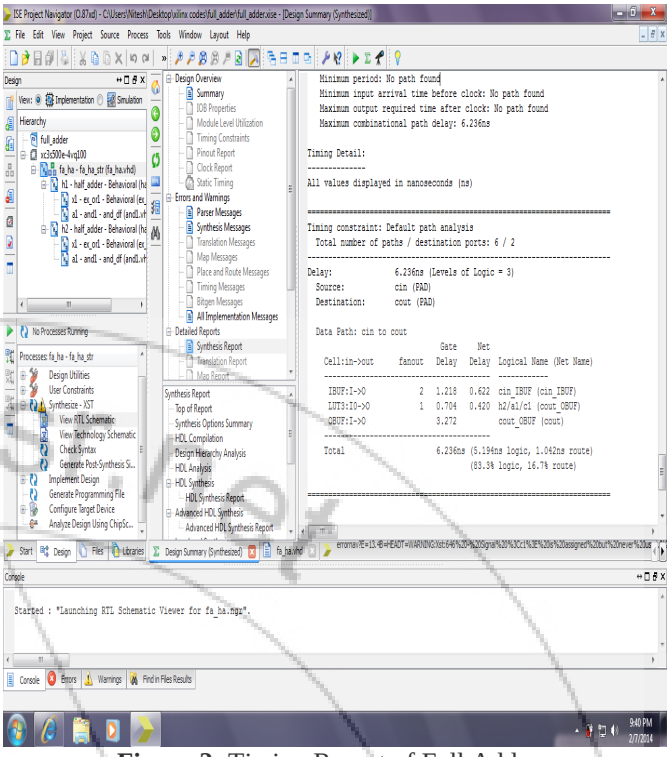

Figure 2: Timing Report of Full Adder

Then again improved the code with VID technique and compare the timing results of both. The power optimization is a main component in low power design with CMOS devices which achieved with the VID technique.

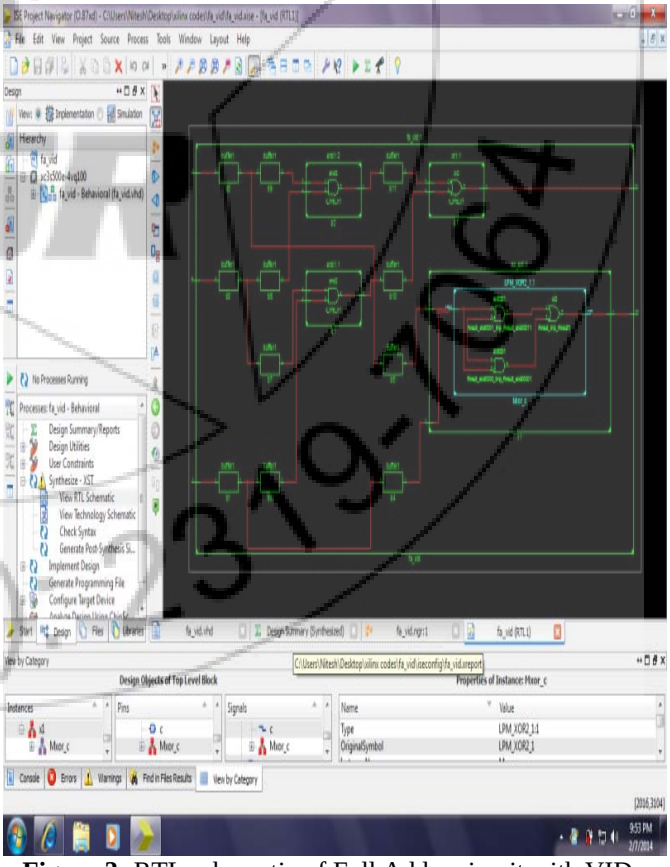

Figure 3: RTL schematic of Full Adder circuit with VID concept

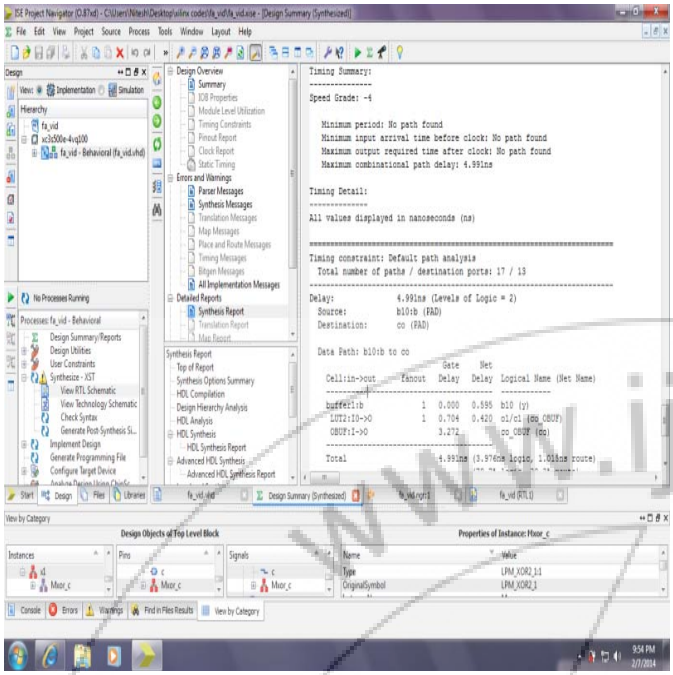

Figure 4: Timing Report of Full Adder using VID concept

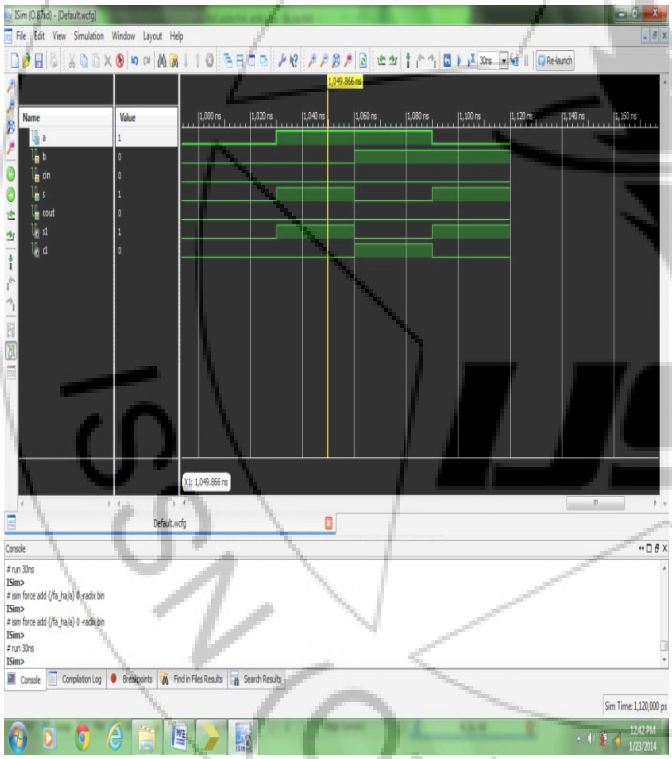

Figure 5: Simulation results of Full Adder circuit

RTL schematic and timing report of both conditions given by figures. After compare the timing report of both conditions we get optimized Full adder circuit with 50% of power.

5. Conclusion

This paper considered the VID technique for reduction of dynamic power in CMOS logic circuits. There is Full adder circuit implemented using VID technique which gives better result. 50% of power optimized in the circuit. This technique used buffer insertion at critical path delays which reduced the delay of these paths. With this technique the area increased due to buffer insertion so technique can be modified with area improvement.

6. Acknowledgment

I would like to express by deep gratitude and thanks to Dr. Mahesh Bundele, Coordinator and Research, in Poornima University and my Guide Mr. Sanjay Sharma, for giving me an opportunity to work under his guidance.

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