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Analysis and Simulation of Multilevel DC-link Inverter Topology using Series-Parallel Switches

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Abstract: ***This paper deals with a multilevel dc-link inverter topology with reduced number of series-parallel switches [1]. A large electrical drives and utility application demanding advance power electronics converter to meet a great power requirement [11]. As finding result multilevel power converter structure has been import as a high power and medium voltage situations. A multilevel inverter not only obtaining high power rating but also become better performances of system in relative to harmonics. In this paper modified inverter can get output more numbers of voltage levels with less numbers of switches(which connect in Series-Parallel) as comparable to cascaded H-bridge inverter which results in reduction of installation cost & easy to controlling .The circuit methodology, theoretical description and Matlab based simulation results described in detail in this paper.***

Keywords: H-bridge, PWM, Switched series-Parallel, THD.

1. Introduction

A multilevel inverter is a power electronic system that produce a desired output voltage from several levels of dc voltages inputs. Recently, multilevel power conversion technology has been developing the area of power electronics very fastly with good potential for future advancement growth. The most attractive applications of this technology are in the medium to high voltage ranges. The multilevel inverter (MLI) is used for high voltage and high power applications. This inverter make staircase (stepped) waveform from several different levels of DC voltage. It have inferior voltage rating of devices, low harmonics distortion, high power quality waveforms, lower switching frequency and losses, higher efficiency, reduction of dv/dt stresses. Because of the above characteristics, it have a prospect of working with low speed semiconductors if its compared with the two level inverters. Many number of MLI topology are available but generally popular MLI topology is diode clamped, flying capacitor and cascaded multilevel Inverter.

Diode clamped MLI used in fans; conveyors, and robust applications, one application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line [2]. Another application would be as a variable speed drive for high-power medium-voltage (2.4 kV to 13.8 kV) motors as proposed[3,11],Efficiency is high for fundamental frequency switching, a voltage unbalancing problem occurred in diode clamped MLI, on the other hand Flying capacitor[5] used in back to back configuration for regenerative system, Real and reactive power flow can be controlled Control is complicated to track the voltage levels for all of the capacitors Switching utilization and efficiency are poor for real power transmission[10,11], a pre voltage initialization across capacitors necessary for this type of MLI. but Cascaded H-bridge MLI can used for high voltage& power rating.[4,7]

The major disadvantage of Cascaded H-bridge MLI is consisting more numbers of switches (for gaining one more level, switches increased linearly by four) and switching losses get increased[9]. So switching losses have affected the output voltage and overall efficiency also.

The Modified Inverter topology gives more number of voltage level using less number of switches. The modified inverter topology has also improved the THD.

2. Circuit Description

In Modified MLI ,there are two parts, one part is H-bridge with a single DC source and another part is an inverter circuit which connected in cascaded. In second part of modified MLI the DC voltage source in inverter circuit is in parallel by various combination of switches[1]. The DC voltage source of H-bridge inverter is V_0, i.e. independent on another inverter circuit voltage V_k (k = 0,1,2…..n).

We assuming a fix ratio for various voltage levels $V_0 : V_k$ (k = 0,1,2……n). such as an example for 15-level 1:3 ratio assumed. DC voltage source with switches (Sa-San_1 & Sb-Sbn_1) can extendable for higher number of level, taken assuming a changeable value of fix ratio. In conventional CHB there are 12 switches used for 11 level & 16 switches with hybrid modulation technique on other hand only 11 switches used for 11 level, 14 switches for 15 level assuming 1:2 ratio in modified topology. There are 11 switches used for 15 level assuming 1:3 ratio in modified topology and 12 switches used in conventional MLI.

A basic formula can obtain for multilevel on basis of analysis is:

$$N= 4n+3$$

The structure circuit diagram is shown in fig.1. In the circuit analysis the dc voltage source can be connected in series and parallel connection by different combination of switches. In fig. 1 voltage source connect in both way, we already know that in parallel connection, equivalent voltage can be equal to voltage, when parallel voltages have equally, so when switch Sa1 will OFF and switch Sb1 &

Sc1 is in ON state dc voltage sources is in parallel combination. When switch Sa1 is ON, voltage source is in series connection. Both parallel switches having same gate pulses.

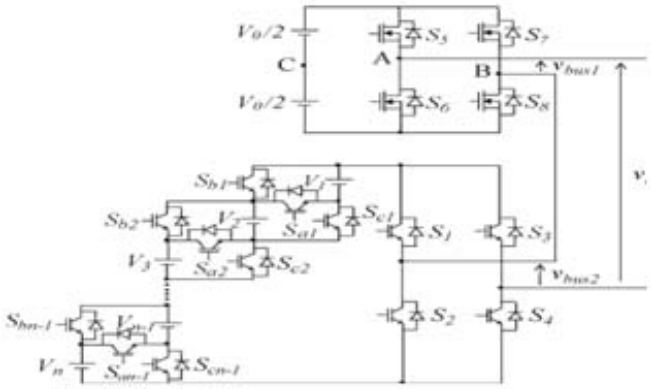

Figure 1: Structure of the modified (4n+3) level inverter with series-parallel connected switch

But in fig. 2 only dc series connection is possible because there is an absence of a switch to be a parallel connection. So series connection has same output level with reduced switch, low switching loss has occurred. In this connection method only 10 switches used for 11 level, 12 switches for 15 level assuming 1:2 ratio in circuit topology. Here only 10 switches used for 15 level assuming 1:3 ratio in modified topology and 12 switches used in conventional MLI. In this paper we discuss about only dc voltage series combination. In this circuit we used IGBT switch only at place of MOSFET to reducing switching loss.

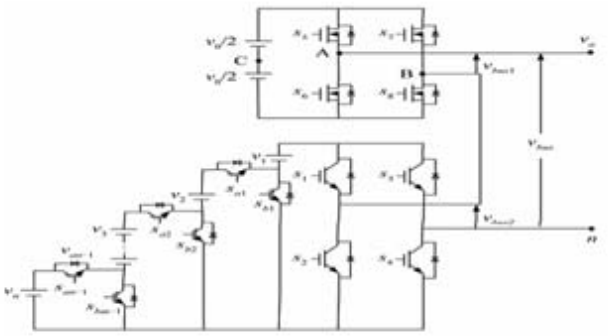

Figure 2: Structure of the modified (4n+3) level inverter with only series connected switch

One more thing if we don't have reverse power flow in circuit, replacing IGBT (Sb-Sbn_1) switches by diodes. For a resistive load both current & voltage are in same phase, so no reverse power flowing but in case of RL load output current lags voltage and having chances to reverse power flowing, in such case IGBT replaced by diodes. In this modified topology, we take assuming a 1:3 ratio for 15 level.

Table 1: Comparison between different topology for 15 level MLI.

MLI type	*Cascaded H-bridge*	*Diode clamped*	*Flying capacitor*	*Modified MLI*
IGBT	*28*	*28*	*28*	*10*
Bypass diodes	-	-	-	-
Clamping diodes	-	*24*	-	-
DC split capacitors	-	*6*	*6*	-
Clamping capacitors	-	-	*12*	-
DC source	*7*	*1*	*1*	*3*
Total	*35*	*59*	*47*	*13*

3. Circuit Operation

In fig. 3 the basic structure of 15 level modified MLI shown. There are two cycles (+ve & -ve) by which 15 level output voltage obtained. The whole operation phenomenon shown in table 2 and table 3.

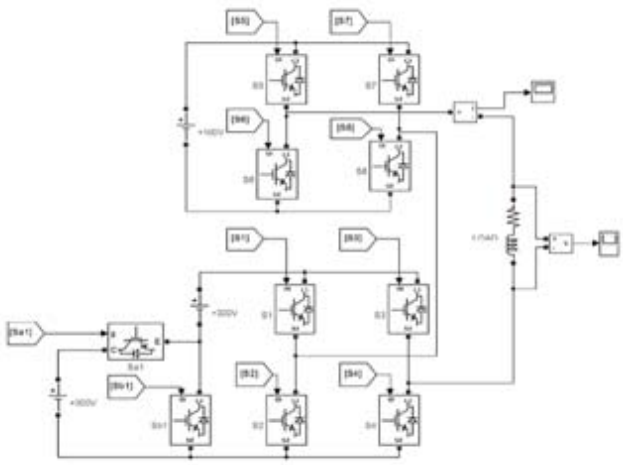

Figure 3: Basic structure of 15 level modified inverter

Table 2: Operation of +ve mode 15 level modified topology

Operating Modes	*Current Paths*
Level-1 (+Vdc)	*+Vo→S5→Load→S4→S2→S8→ -Vo*
Level-2 (+2Vdc)	*+V1→S1→S7→Vo→S6→Load→S4→Sb1→-V1*
Level-3 (+3Vdc)	*+V1→S1→S8→S6→Load→S4→Sb1→ -V1*
Level-4 (+4Vdc)	*+V1→S1→S8→Vo→S5→Load→S4→Sb1→-V1*
Level-5 (+5Vdc)	*+V2→Sa1→V1→S1→S7→Vo→S6→Load→S4→ -V2*
Level-6 (+6Vdc)	*+V2→Sa1→V1→S1→S8→S6→Load→S4→-V2*
Level-7 (+7Vdc)	*+V2→Sa1→V1→S1→S8→Vo→S5→Load→S4→ -V2*

Table 3: Operation of -ve mode 15 level modified topology

Operating Modes	*Current Paths*
Level-8 (0Vdc)	*S2→S8→S6→Load→S4*
Level-9 (-Vdc)	*+Vo→S7→S2→S4→Load→S6→-Vo*
Level-10 (-2Vdc)	*+V1→S3→Load→S5→Vo→S8→S2→ Sb1→-V1*
Level-11 (-3Vdc)	*+V1→S3→Load→S6→S8→S2→Sb1 →-V1*
Level-12 (-4Vdc)	*+V1→S3→Load→S6→Vo→S7→S2→ Sb1→-V1*
Level-13 (-5Vdc)	*+V2→Sa1→V1→S3→Load→S5→Vo →S8→S2→-V2*
Level-14 (-6Vdc)	*+V2→Sa1→V1→S3→Load→S6→S8 →S2→-V2*
Level-15 (-7Vdc)	*+V2→Sa1→V1→S3→Load→S6→Vo →S7→S2→-V2*

4. Modulation Strategy

There are different types of modulation techniques used in MLI for generating gate pulses. In Modified MLI we are using Phase disposition pulse width modulation scheme, in which multi carrier waves have in phase [6]. PD waveforms for modified inverter are shown in fig.4. PWM technique used in MLI because it better control the output voltage, regulate the output voltage and control the harmonics presented in the output voltage. We know that for N –level output N-1 carrier waves are used. All carrier signals have same frequency [10].

Two parameters, which is used in PWM scheme with related to harmonics known as Modulation index &Frequency modulation ratio. Modulation index is defined as the ratio of amplitude of reference signal to carrier signal.

$$m_a = \frac{A_{ref}}{(N-1)A_{carr}} \quad (1)$$

Where N is no. of voltage level

$$V_{omax} = m_a V_{dc} (m_a \leq 1) \quad (2)$$

If Modulation index reduces, harmonic components gets increased so modulation index having maximum value (m_a=1) as possible to overcome this problem.

Another parameter Frequency modulation ratio is defined as ratio of frequency of carrier signal to reference signal. Harmonic components presents in output voltage as function of m_f,

$$m_f = \frac{f_{carr}}{f_{ref}} \quad (3)$$

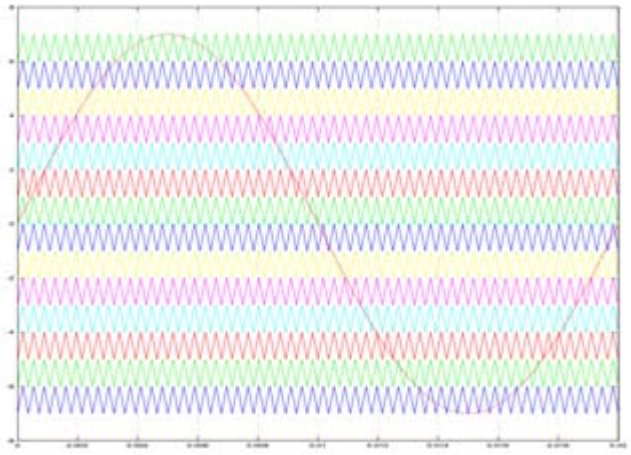

Figure 4: PD modulation scheme with reference and multi carrier signals

A reference sine wave is compared with multi carrier waves with relational operator. In proposed 15 level MLI, 14 carrier generators are used and compare it with reference sine wave finding different comparable pulses are combined by an adder and then it would again comparing with different constant values (0-14), after this obtaining various pulses we have grouping different pulses with EX-OR logic gates for selecting exact controlling signal to switches .The gate control circuit is heart of any multi-level inverter. The switching circuit is shown in figure 5.

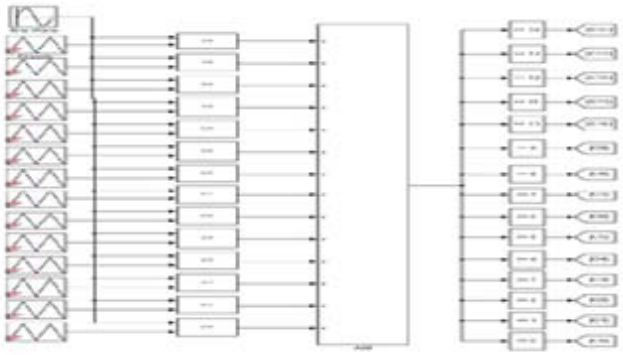

Figure 5: Comparator circuit of 15 level modified MLI

Table 4:.Digital combinational table for switching pulses

SWITCH	*DIGITAL PROCESS (× shows EX-OR operator)*
S1	*C0×C1×C2×C3×C4×C5*
S2	*S1 Connect with NOT gate*
S3	*S4 Connect with NOT gate*
S4	*S1×C6×C7×C8*
S5	*S8×C0×C3×C6×C7×C9×C12*
S6	*S5 Connect with NOT gate*
S7	*C2×C5×C7×C8×C12×C14*
S8	*S7 Connect with NOT gate*
Sa1	*C0×C1×C2×C12×C13×C14*
Sb1	*S1×C0×C1×C2×C9×C10×C11*

Where C0-C14 is constant comparable pulses and S1-Sb1 is main switches.

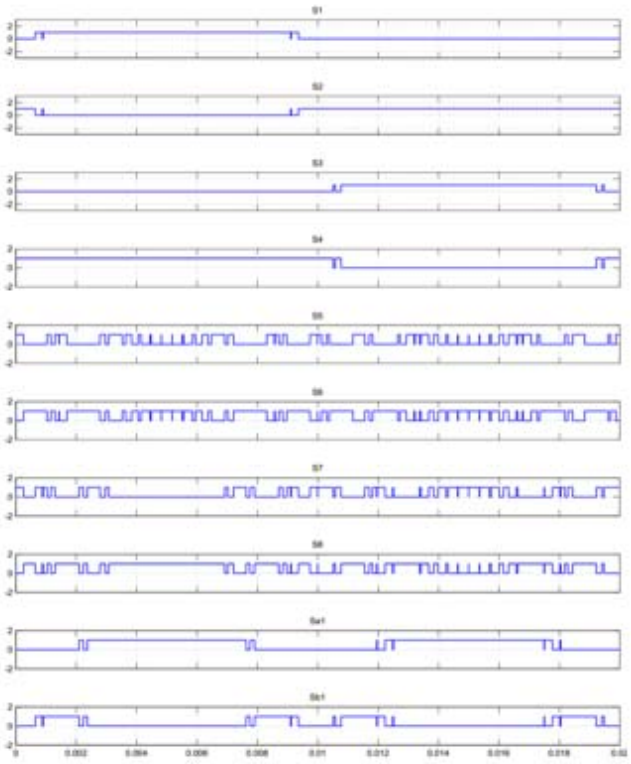

Figure 6: Firing pulses for switches

5. Simulation Result

Under this subpart, simulation result of the 11& 15 level modified MLI is synthesized using MATLAB 2013a. Load parameters taken R=3 ohm &L=6 mh.

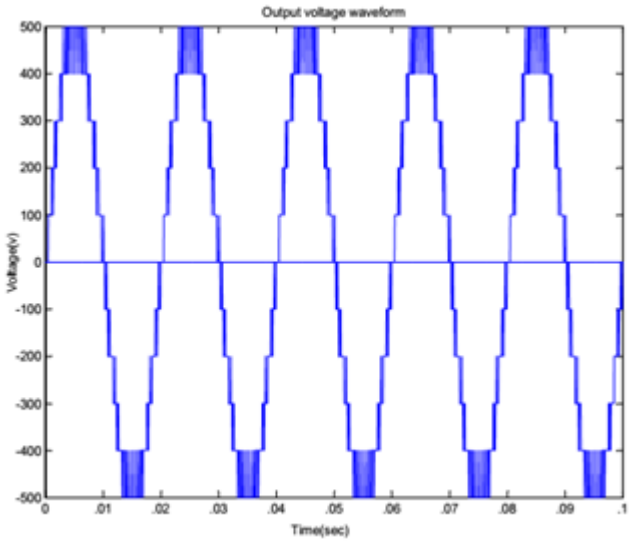

Figure 7: simulated output voltage for 11 level modified MLI

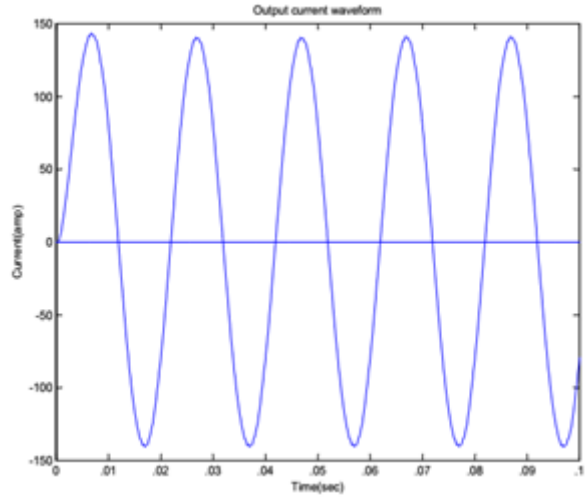

Figure 8: simulated output current for 11 level modified MLI

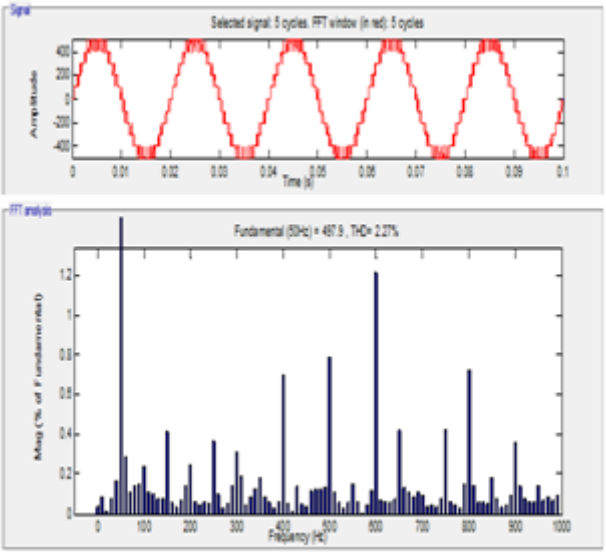

Figure 9: FFT window for 11 level o/p voltage

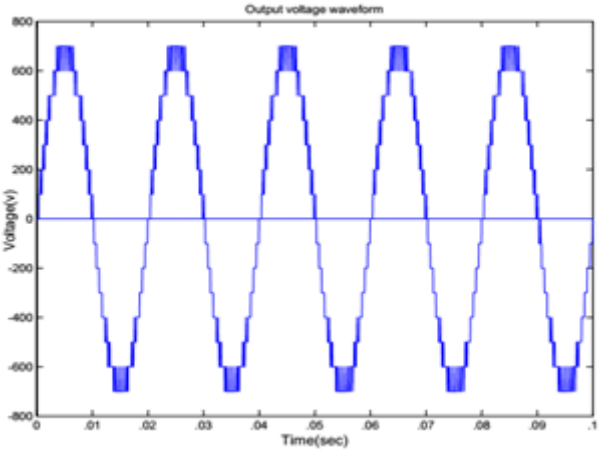

Figure 10: simulated output voltage for 15 level modified MLI.

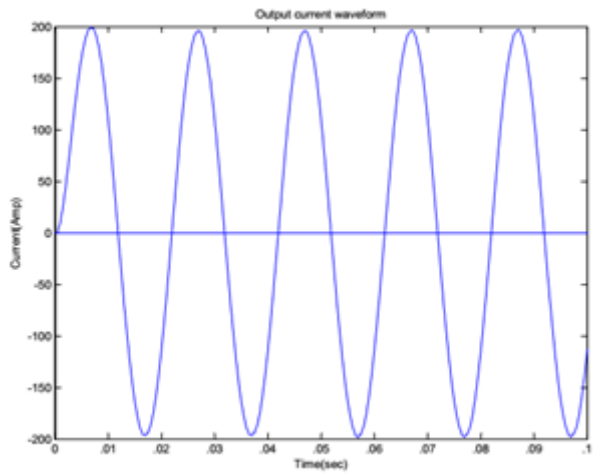

Figure 11: simulated output current for 15 level modified MLI

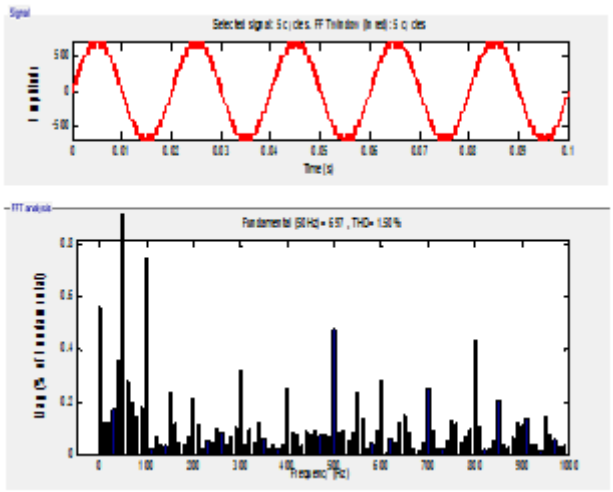

Figure 12: FFT window for 15 level o/p voltage

6. Conclusion

The modified multilevel inverter has obtained low harmonics content, low switching losses, high power and high output voltage level. It has used less number of switches as compare to conventional inverter. In this circuit we used IGBT switch only at place of MOSFET to reducing switching loss. Modified inverter has simulated at various modulation index. In this paper we have comparative study on 11 level & 15 level at different modulation index. This topology obtained 1.50% THD at modulation index 1 at fundamental max frequency. So this topology has low power consumption and having less size.

Table 5:.Comparison of THD between 11& 15 level at different modulation index

Modulation index	*THD(11 level) %*	*THD(15 level) %*
1	*2.27*	*1.50*
0.97	*2.10*	*1.58*
0.95	*2.04*	*1.75*
0.90	*2.45*	*1.79*

7. Future Improvement

There are many future scope improvements in this study like reducing THD using various PWM techniques. For taking low ON time period to generating multilevel outputs. Uses a LC type filter to obtaining smooth voltage & Current waveforms.

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