

# Design of Multimode Deinterleaver for different Wireless Communication Standards

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**Abstract:** *The advancement in communication systems has reached a new level with the development of wireless devices. The data stream to be transferred has to undergo different error correcting techniques to ensure better reliability and security. Interleaving is a basic method to reduce the effect of burst errors. It is mostly implemented by permutation tables and complex mathematical equations. This paper presents a simple and robust architecture for address generation of deinterleaver used for different wireless communication standards. In order to reduce the silicon cost, hardware multiplexing is introduced. The traditional LUT based address generation is found to be unattractive in many aspects such as large sequential memory requirement, slowness in operation and enormous power consumption. The proposed design is capable of sharing the common hardware between the modules for band phase shift keying (BPSK), quadrature phase-shift keying (QPSK), 16-QAM, and 64-QAM. The algorithm for address generator of the deinterleaver is simplified and simulation results are provided in this paper. This novel technique supports each modulation scheme at different possible code rates. This work uses a finite state machine based architecture to generate addresses which contributes to adequate use of resources. With the increase in bandwidth requirements for communication, it has become necessary to include an address generation technique used for WLAN 802.11n in this work. The comparison between conventional method and proposed technique is made on the basis of power rating and equivalent gate count estimated using Xilinx ISE tool.*

**Keywords:** Wireless communication standards, Deinterleaver, Hardware multiplexing, Finite state machine, Address Generator

## 1. Introduction

Wireless communication is a fastest growing segment of the communications industry. It is a process of transferring information between two points when they are not connected by an electrical conductor. The need for wireless communication increases with the growing demand for internet access, driven by web browsing and email exchange. The key to the success of broadband wireless access is to offer a solution which is reliable and easy to deploy compared to the competitive copper technologies. The explosive growth of wireless systems coupled with the proliferation of laptop and palmtop computers indicate a vibrant future for wireless networks, both as stand-alone systems and as part of the larger networking infrastructure. The key advantages of wireless networks as opposed to wired networks are mobility, flexibility, ease of installation and maintenance.

Wireless Local Area Network (WLAN) links two or more devices using a wireless communication method. It can be considered as a group of wireless access points and associated infrastructure established in a geographic area, like an office building or campus, which is capable of radio communications. Wireless LANs designed to operate in different license-free bands making their operation and maintenance costs less than contemporary cellular and PCS networks. IEEE 802.11n is an amendment that improves upon the previous 802.11 standards by adding multiple-input multiple-output antennas (MIMO). 802.11n operates on both the 2.4 GHz and the lesser-used 5 GHz bands. This technology can provide mobile users with a network that

supports a broad range of mobility applications without compromising total network performance.

WiMAX [2] is a recent wireless broadband standard that has promised high bandwidth over long-range transmission. WiMAX is an acronym for "Worldwide Interoperability for Microwave Access" (WiMAX). This wireless digital communications system, also known as IEEE 802.16, is intended for wireless "metropolitan area networks". WiMAX can provide broadband wireless access up to 30 miles (50 km) for fixed stations, and 3 - 8 miles (5 - 12 km) for mobile stations. At the same time, the WiFi is limited in most cases to only 150 - 300 feet (30 - 100m). WiMAX is capable of providing a spectral efficiency of 5 bps/Hz, which is very good compared to other broadband wireless technologies.

The primary role of an interleaver is to disperse the sequences of bits in a bit-stream in order to minimize the effect of burst errors introduced in transmission. An interleaver is used in conjunction with some type of error correcting code. It is placed between the encoder and the transmitter whereas deinterleaver is between the receiver and the decoder. The error correcting codes is used to correct the lost information as long as the amount of lost bits in a single codeword is within the limit. The data stream to be transmitted in the wireless communication medium contains some errors and distortion. In order to obtain the exact sequence of data at the receiver, it should be randomized. Channel coding [4] can be described as the process of transformation of signals to improve communications performance by increasing the robustness against channel impairments such as noise, interference and fading. The coding is carried out on the data sequences by altering the

characteristics of the sequences. The converted sequences exhibits a structured redundancy that initiates a decision process, by a transmitter or a receiver, less subject to errors. The purpose of the modified data is to convert the sequences of 1's and 0's in a random sequence to improve the coding performance. The major component of the data randomization is Pseudo Random Binary Sequence generator which is implemented using Linear Feedback Shift Register. The Reed-Solomon code is used with the data to add redundancy to the data sequence. This helps in correcting block errors associated with the signal.

Orthogonal Frequency Division Multiplexing [5] is an elegant and efficient scheme for high data rate transmission in a non-line-of-sight or multipath radio environment. OFDM belongs to a family of transmission schemes called multicarrier modulation, works on the idea of dividing the high bit-rate data stream into many parallel lower bit-rate streams and each modulated stream is on separate carrier—often called subcarrier, or tone. Here the subcarriers are selected in such a way that they are all orthogonal to one another over the symbol duration. It avoids the need to have non-overlapping subcarrier channels to terminate the interference. OFDM facilitates coding and interleaving across subcarriers and provide improvement against burst errors. In fact, WiMAX/WLAN defines subcarrier permutations that allow systems to exploit this multiplexing. Different types of interleavers [3] are used at the receivers of the communication system. Those are random, S-random and relative-prime interleavers. Random interleaver is the raw interleaver generated through randomly selecting the addresses over a range of block size. They do not bear any structure and the main disadvantage is that once generated through some random function, they cannot be reproduced as such. In other words, the random interleavers do not guarantee sufficient information spread. To avoid this situation semi-random interleaver named as S-random interleavers are introduced. This interleaver ensures a distance according to the required function between two adjacent carriers. Relative prime interleavers provide higher spread, and especially they are good for short block sizes. They are considered to be easier to implement as compared to random and S-random interleavers.

Look Up Table [6] based address generation technique is a complex and conventional method. Each modulation scheme requires a separate LUT causes more space and power. Four LUTs are required to store the interleaver addresses of four modulation schemes of a communication standard. In order to generate proper address for different standard, another LUT has to be used. For interleaving, the input bits are written sequentially and are read in the order defined by the LUT. For deinterleaving the bits are written according to the LUT and then read sequentially.

Another method of address generation used for interleaving the data bits is 2-D realization [11] of the interleaver. This method is better than previous LUT based technique because the conventional method uses memories for storing the permutation tables which is silicon consuming. This silicon cost of the permutation tables for interleaver implementation used in the conventional approaches can be very high if the

device is supporting many variants inside a particular standard. Due to the presence of complex functions like floor function and modulo function, the implementation of the two steps of permutations by direct computation are found to be quite hardware inefficient. A low complexity technique of generating address based on finite state machine architecture is proposed for WLAN [9]. This supports all the modulation schemes, varying interleaver depths (ID) and different code rates. Any change in the value of ID or modulation type prompts the interleaver to follow a different path or else the FSM will follow the same route of transition and the same set of interleaver addresses will be continuously generated. When the FSM at this level reaches to the terminal value of that iteration, it goes to the preset state in order to continue the process. Preset state/ Preset Logic is used to generate the correct beginning addresses. This method can be easily implemented on hardware with minimum area and power consumption. The change in modulation scheme or code rate causes a transition from one state to other. In this paper, we propose a simple architecture for address generation that can be used for multimode deinterleaver. This design provides a common platform for WLAN, IEEE 802.11n and WiMAX. The modulation schemes supported are BPSK, QPSK, 16-QAM and 64-QAM at different code rates.

The rest of the paper is organized as follows: Section 2 contains the interleaving technique in wireless communication system. Section 3 describes the multimode block interleaver architecture. The proposed design for address generation is discussed in section 4. Simulation results are presented in section 5. This brief is concluded in the final section.

## 2. Interleaving in Wireless Communication System

The basic communication system mostly consists of an information source (producing a message or sequence of messages), a transmitter (having the capability to operate on the message to convert it to a suitable signal for transmission), a channel (a medium like air or wire etc.), a receiver (practically inverse of transmitter operations), and the destination (a person or a machine). The noise source can be defined as burst noise (lightening, switch noise), white noise, or channel distortion. Interleaver is used to reduce the effect of burst errors.

The usual sources of burst errors are listed below:

- Channel distortion and channel fading effects in wireless communications
- Lightening and switching effects
- Use of concatenated coding schemes

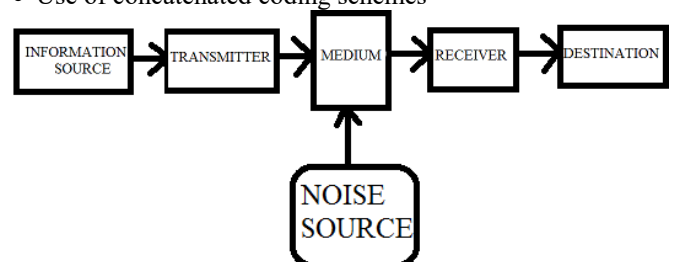


Figure 1: Basic Communication system model

A basic interleaver is taken as a sequential device with single input and single output. A parallelism can be devised but the basic function remains the same [3]. The interleaver takes a sequence of information bits with fixed width and generates another sequence of same width but in different order. It is then the role of a de-interleaver to retrieve back the original order. Thus the interleaver and deinterleaver strictly work as a team to ensure efficiency.

A general interleaver should be able to carry out the following steps:

- 1) Bits are written to matrix row by row.
- 2) Intra-row permutations are performed.
- 3) Intra-column permutations are performed.
- 4) Bits are read column by column.

Different interleaving patterns apply for different modulation schemes BPSK/QPSK, 16-QAM and 64-QAM [3]. The channel interleaving is based on a block interleaver, which is expressed in the form of two equations for different steps of permutations. The interleaver specified in WLAN, 802.11a/b/g also utilized same type of permutation steps; therefore, the proposed work can also cover WLAN as well as WiMAX by default. The block interleaver/ deinterleaver exploit different depths of  $N_{cbps}$  to incorporate various code rates and modulation schemes for different wireless communication standards. The data stream received from the encoder is permuted by using the equations (1) and (2). The first equation maps the adjacent coded bits to non adjacent subcarriers. In the second equation, the adjacent coded bits are mapped alternately to more or less significant bits of the constellation to eliminate the long run of lowly reliable bits. Thus,

$$m_k = (N_{cbps}/d) \cdot (k \% d) + [k/d] \quad (1)$$

$$j_k = s \cdot [m_k / s] + (m_k + N_{cbps} - [d \cdot m_k / N_{cbps}]) \% s \quad (2)$$

Here  $N_{cbps}$  is the block size corresponding to number of coded bits per allocated sub-channels and the value for  $d$  used in WiMAX/WLAN is 12 and 16. The value of  $d$  represents the number of columns of the block interleaver. The operator  $\%$  is defined as the modulo function [5].  $m_k$  and  $j_k$  are the outputs after implementing the first and second equations, respectively; and the value of  $k$  varies from 0 to  $N_{cbps} - 1$ .  $s$  is defined as half of  $N_{pc}$ , i.e.  $N_{pc}/2$ . The  $N_{pc}$  is the number of coded bits per subcarrier, i.e., 1, 2, 4, or 6 for BPSK, QPSK, 16-QAM, or 64-QAM, respectively. Modulo is signified by percent.

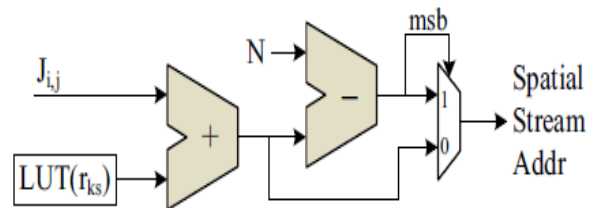
Two permutations, i.e., (3) and (4) defines the deinterleaver, which performs the inverse operation. Let  $m_j$  and  $k_j$  define the first and second level of permutations for the deinterleaver, where  $j$  is the index of received bits within a block of  $N_{cbps}$  bits. Thus

$$m_j = s \cdot [j / s] + (j - [d \cdot j / N_{cbps}]) \% s \quad (3)$$

$$k_j = d \cdot m_j - (N_{cbps} - 1) \cdot [d \cdot m_j / N_{cbps}] \quad (4)$$

The frequency interleaving makes a continuous wideband signal by summing multiple narrower hand signals that overlap in frequency. IEEE 802.11n is a wireless networking standard that makes use of multiple antennas to increase data rates with the help of four spatial streams. The interleaving

requires frequency rotation in the case when more than one spatial stream is transmitted. The frequency rotation is applied to the output of the permutation equations. The parameters are used to define different frequency rotations for 20 MHz and 40 MHz case in 802.11n. The frequency rotation also depends on the index of the spatial stream, thus each spatial stream faces different frequency rotation. As the rotation is fixed for a specific spatial stream, the starting value also holds for all run time computations. A lookup table can be used for the starting values for different spatial streams. Therefore, the frequency rotation can be computed with a very small hardware as shown in Figure 2.



**Figure 2:** Schematic circuit for frequency rotation in 802.11n

The information content from multiple bands is combined together to create continuous wideband signal with arbitrary spectral content. The overlap removes the redundant information.

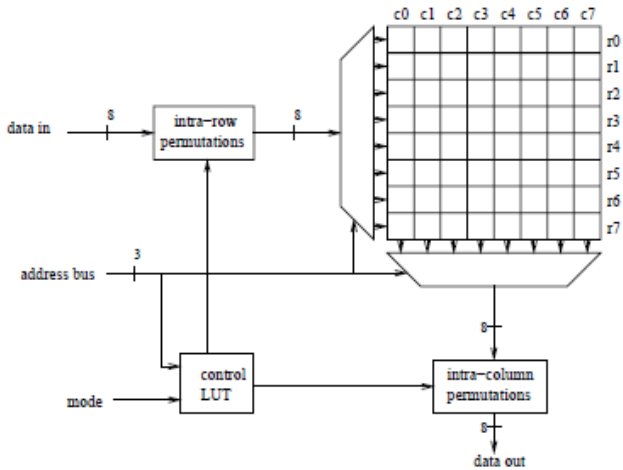
### 3. Multistandard Block Interleaver Architecture

The multistandard block interleaver is used to avoid the necessity of addressing each individual bit in the memory and by enable the read and write of multiple bits in parallel [8]. The main disadvantage of traditional block interleaver is that the bits have to be written and read one at a time. Another disadvantage of traditional method is that a complete interleaving sequence of each interleaving scheme has to be stored explicitly in different Look Up Tables, making it relatively large if multiple modes have to be supported.

The multistandard block interleaver architecture is more suitable for operation as an accelerator unit for a programmable processor. It should therefore be possible to make the interleaver compatible with the processor word length.

Ideally the interleaver interface to the processor should look like an ordinary memory. Then the interleaver is also used as a normal data buffer and it would be possible to carry out the interleaving at no extra instruction cost. The number of rows and columns should be configurable. The solution should be suitable for multiple standards, i.e. multiple intra-row and intra-column permutation schemes should be supported. It might not be a general platform but the cost for supporting additional modes can be reduced compared to the corresponding cost (for increasing ROM size) in the traditional approach. The architecture is based on a special matrix memory block where words are written as rows but

read as columns. The figure 3 shows the block diagram of multi-standard interleaver.



**Figure 3:** Block Diagram of Multi-standard block interleaver

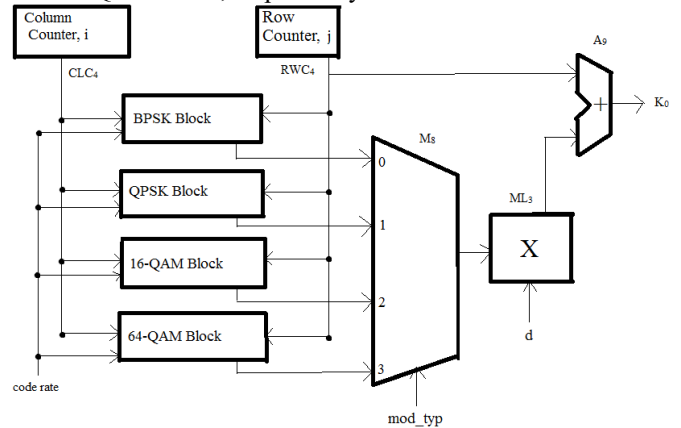
A complete row can be written in one clock cycle and a complete column can be read [10]. Intra-row permutations are carried out before the bits are stored to memory by reordering the bits available on the input data bus. Similarly, intra-column permutations are performed by reordering the bits on the output data bus after the data has been read. If different permutation schemes are required, the permutation blocks are implemented as a set of small multiplexers using the same control signal. By this architecture, it is easy to interleave a block of R rows and C columns in R + C clock cycles, since both R and C are smaller than the longest word length of the processor compared to the traditional method which needs  $2 * R * C$  cycles.

A considerable part of the area in the old architecture is occupied by the LUT, which needs one entry per bit. The hardware used in the new architecture only needs one entry per row and column to store permutation modes [7]. This means that the extra area for each scheme that needs to be implemented is much smaller in the multistandard architecture than previous methods because the permutation blocks become smaller. The new architecture needs more memory cells than the traditional one, but since rows/columns that are not needed are deactivated so the number of active memory cells are the same in both solutions. Since the multistandard architecture completes the interleaving in fewer clock cycles, it can execute at a lower clock frequency. This helps to reduce power consumption by lowering the supply voltage.

#### 4. Proposed Design for Address Generation in Deinterleaver

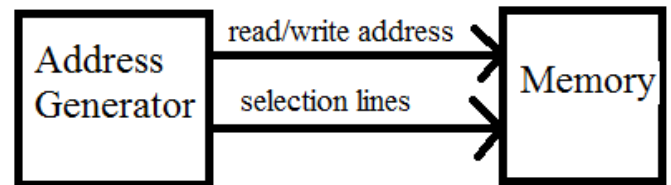
This paper presents a novel technique to implement the address generator of interleaver which is capable of operating in four different modulation schemes such as BPSK, QPSK, 16-QAM and 64-QAM for WLAN, IEEE 802.11n and WiMAX . This proposed technique comprises of hardware multiplexing and finite state machine (FSM) based address generator. The top-level structure of the deinterleaver address generator is shown in figure 4. The logic circuits are

presented here as BPSK block, QPSK block, 16-QAM block, and 64-QAM block, respectively.



**Figure 4:** Block Diagram of proposed technique

Address generation is the primary concern for all types of interleaving. The proposed hardware model of the interleaver consists of two sections: address generator and interleaver memory as in figure 5. The address generator is basically the simultaneous implementation of (1) and (2) which is the write address along with provision for generation of read address for interleaver memory. The role of address generation block is to generate non-overlapping addresses for the interleaver within a specific pattern.



**Figure 5:** Generalized view of interleaver architecture

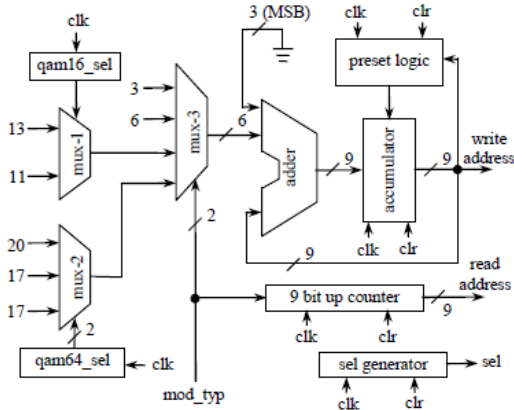
In our design, the addresses are generated in a specific manner for different modulation schemes for each wireless communication standard. The addresses for BPSK and QPSK modulations are generated at linear spacing of values 3 and 6 respectively. These follow a pattern of multiples of 3 for BPSK and 6 for QPSK for initial addresses. Similarly the 16-QAM modulation exhibits a non-linear pattern of 13 and 11 alternatively. For 64-QAM, the address are generated at a spacing of 20, 17 and 17 alternatively.

BPSK	0	3	6	9	12	15	18	21
	24	27	30	33	36	39	42	45
	1	4	7	10	13	16	19	22
	25	28	31	34	37	40	43	46
QPSK	0	6	12	18	24	30	36	42
	48	54	60	66	72	78	84	90
	1	7	13	19	25	31	37	43
	49	55	61	67	73	79	85	91
16-QAM	0	13	24	37	48	61	72	85
	96	109	120	133	144	157	168	181
	1	12	25	36	49	60	73	84
	97	108	121	132	145	156	169	180
64-QAM	0	20	37	54	74	91	108	128
	145	162	182	199	216	236	253	270
	1	18	38	55	72	92	109	126
	146	163	180	200	217	234	254	271

**Figure 6:** Write addresses for four different modulation schemes

The schematic diagram of the address generator is given in the figure 7. The design contains three multiplexers, an adder, an accumulator and a counter. The mux-1 is used to

implement the sequences for 16-QAM where as mux-2 is used for 64-QAM. The outputs of mux-1 and mux-2 are fed to the mux-3. The increments for BPSK and QPSK are also provided as inputs of mux-3. The bits of mod\_typ signal choose the required modulation scheme. The output of mux-3 is one of the inputs of adder. The 6-bit output of mux-3 is zero padded to 9-bits. The accumulator is controlled by a finite state machine based preset logic. The other input of adder is the previous address generated by the system. A simple 9-bit counter is used to the read the addresses.



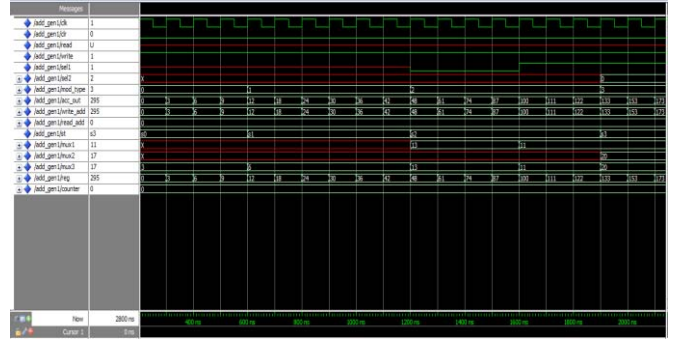
**Figure 7:** Schematic diagram of address generator

The preset logic is the heart of address generator, shown in figure 8. The principal function of finite state machine is to generate the correct beginning write addresses for all subsequent iterations. The controlled finite state machine operates in two modes, say, pre-computation mode and execution mode. In pre-computation mode, it determines the necessary parameters and initializes the registers. During the execution phase, the preset logic also keeps track of block size by employing row and column counter, thus providing the block synchronization required for each type of interleaver implementation.

The modulation scheme is determined by the value of state of finite machine. Each state is used to represent a modulation scheme for communication standard. At the initial phase (if clr=1), the fsm enters first state with initial values of parameters. With each increment, the modulation scheme differs. It occurs like s1 for BPSK, s2 for QPSK, s3 for 16-QAM and s4 for 64-QAM. The modulation scheme is changed instantaneously by varying the state of preset logic.

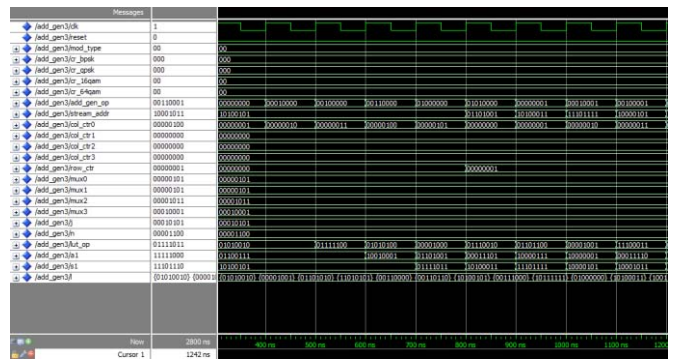
### 5. Simulation Results

The proposed method of address generator used in multimode interleaver for wireless communication systems is simulated using ModelSim Xilinx Edition – III. The hardware logic is converted to VHDL program such that the characteristics can be simulated easily. The figure 8 shows the simulated result of proposed interleaver used for both WLAN and WiMAX. The modulation schemes in this interleaver are BPSK, QPSK, 16- QAM and 64-QAM with different code rates.



**Figure 8:** Simulated result for address generator used for WiMAX and WLAN

The figure 9 shows the simulated result for a common platform which supports WiMAX, WLAN and IEEE 802.11n standards. This displays the finite state machine based address generator output for WiMAX and WLAN. The address generator for the stream addresses are created with the help of a look up table based approach. The outputs are shown separately such that it can be identified easily.



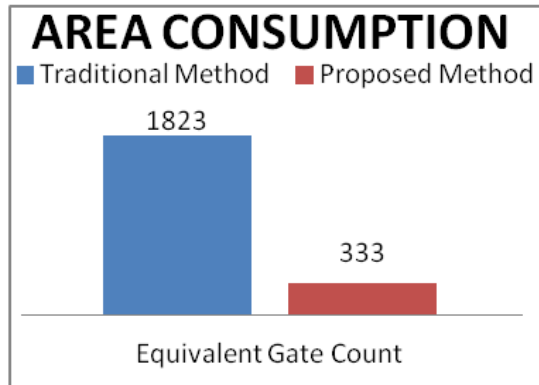
**Figure 9:** Simulated result for address generator used for different wireless communication standards

The combined address generator system utilizes the FPGA resources as 144 slices (2%), 261 flipflops (1%) and 261 four- input look up tables (1%) which is estimated by Xilinx ISE 8.1. This circuit has a power consumption of 232 mW, which shows that it is a low complexity power-efficient technique of address generation for different communication standards.

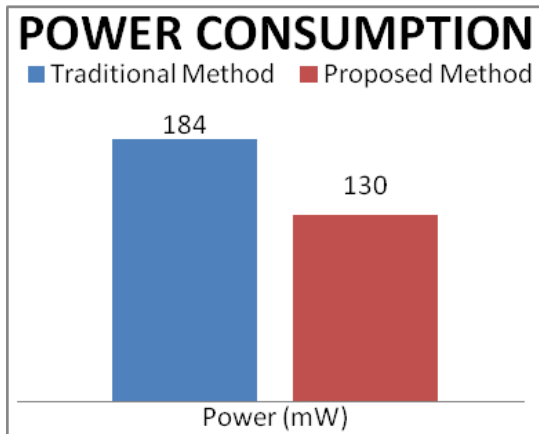
The table 1 shows the comparison of existing method with that of proposed method. From the comparative result, it can be concluded that there is significant reduction in occupancy of the FPGA slices (by 84.76 %), flipflops (by 55%) and four input LUTs (by 87.80%). This comparison clearly proves the low complexity and hardware efficiency of proposed technique over conventional method. A similar comparison with combined address generator platform is not possible because it contains additional part for IEEE 802.11n which is not compatible with existing technique.

**Table 1:** Comparison of resource utilization by two methods

FPGA Parameters	Usage of TRADITIONAL Method	Usage of Proposed Method
Slices	105	16
Flip flops	40	18
4 – input LUTs	205	25
Equivalent Gate Count	1823	333



**Figure 10:** Comparison of area occupied by two methods



**Figure 11:** Comparison of power consumed by two methods

## 6. Conclusion

A novel low complexity finite state machine based address generation technique to model the OFDM based interleaver used in IEEE 802.11a/b/g/n and IEEE 802.16e is proposed. This hardware is able to support all possible code rates and modulation patterns. The hardware implementation is done with the help of VHDL codes. In the presence of a huge range of different block sizes and different types of interleaving patterns, on-the-fly address generation is considered as a bonus feature. Comparison between the proposed work and conventional architecture shows betterment of resource utilization and power consumption.

## 7. Future Scope

Like “space never ends”, research never ends either. In continuation to this work, further research can be done in the area of physical implementation, programmability, and improving the memory sub-system partitioning of the interleaver. A mobile phone being “all-time-partner” of an individual is the most appropriate device to support all different types of communication standards to fulfill the demands. This proposed technique can be enhanced with necessary modifications in algorithm to suit different communication standards. Therefore, the future works should assure reliability in case of address generator which is applicable for various broadband wireless access solutions. Low power consumption and reduced memory usage are primary concerns for the design of interleaver compared to the existing system.

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