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# Modified Reverse Converter in Residue Number System via Specific Hybrid Parallel Prefix Adders

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**Abstract**: ***Residue number system (RNS) is an unconventional non-weighted integer number representation system that uses residues of a number in particular modulus for its representation. Forward converters, modulo arithmetic units, reverse converters are the main part of the residue number system. The reverse converter in the existing residue number system is based on regular and modular adders. It shows significant power consumption and low speed. This is the main reason which prevents the use of Residue Number system in high speed applications. The new reverse converter design method for 4n-moduli set based on the New Chinese remainder theorem. The modified reverse converter design employs the Hybrid-Modular-Parallel prefix-Excess-one modulo ($2^n$-1) adder (HMPE) and Hybrid Regular Parallel prefix Xor/or adder (HRPX). They provide delay and power efficient reverse converter design. The VHDL language is used for coding. Synthesis is done in Xilinx ISE design suite 13.2 and ModelSim SE 6.3f is used for simulation***.

**Keywords:** RNS, Forward converter, Modulo arithmetic unit, Reverse converter, HMPE, HRPX, Modulo adder

## 1. Introduction

Residue number system (RNS) is a non-weighted integer number representation system and uses residues of a number in particular modulus for its representation. It is capable of supporting parallel, carry-free and high speed arithmetic. One of the most important characteristics of the RNS is the limited propagation. Instead of performing arithmetic on a large number, calculations are done in parallel. The major problems in efficient design of RNS are the moduli set selection, forward conversion, residue arithmetic unit, and reverse conversion. Each RNS system is based on a moduli set, which involves a set of pair-wise relatively prime integers. The dynamic range of an RNS system is defined in terms of the product of the moduli, and it denotes the interval of integers exclusively represented in RNS. Forward converter modulo arithmetic unit and reverse converter are the main parts of residue number representation system.

The forward converter decomposes a weighted binary number into a residue represented number with respect to the moduli set. The residue arithmetic unit depends on the application. The reverse converter transforms a residue represented number into its equivalent weighted binary number. But the reverse converter design is more complex and non modular that it compares to the forward converter design. The algorithms of reverse conversion are principally based on the Chinese remainder theorem (CRT), mixed-radix conversion (MRC), and new Chinese remainder theorems (New CRTs). The conversion algorithm resulting equation is simplified by using arithmetic properties. It realized using hardware components like adder, such as carry-save adders (CSAs) and ripple-carry architectures, to implement carry-prefix adders. The usage of the parallel-prefix adders to design reverse converters highly increases the speed at the expense of additional area and power consumption. It makes the reverse converter are more complex. Hybrid specific parallel-prefix adder components are used to provide high speed reverse converter design.

Two important approaches to improve the performance of the reverse converters are 1)Select suitable algorithms , arithmetic properties and propositions for achieve efficient reverse converter design. 2)Introduce new moduli set with large Dynamic Range (DR) for efficient and simple reverse converter design. This two approaches are encourages the RNS based applications.

In reverse converter design the value of moduli of the moduli set must substituted in conversion algorithm formulas obtained from Chinese remainder theorem (CRT), mixed radix conversion (MRC), and new Chinese remainder theorem. The final equation from conversion theorem should be simplified by using some properties.

The absence of carry propagation it leads high speed processing in the RNS based application. Using RNS representation, large number is encoded into smaller numbers. Residue Number System reduces the complexity of the individual arithmetic blocks. This results in power reduction. The RNS is a non-weighted number system with no dependence between its channels. Thus, an error in one channel does not propagate to other channels. So residue number system has less probability of errors. Residue number system can use for reduction in supply voltage, compared to the binary architecture. But division, square-root, sign detection, and magnitude comparison are the difficult operations in Residue Number System. RNS are mainly used in the application.

Forward converters are usually classified into two categories based on the moduli ($2^n$, $2^n$-1,$2^n$+ 1) used. The first category includes forward converters based on arbitrary moduli-sets. These converters are usually built using look-up tables based converter in RNS. The second category includes forward converters based on special moduli-sets. The use of special moduli-sets simplifies the forward conversion process and architectures [4]. ($2^n$, $2^n$-1,$2^n$+ 1) is one of the special

moduli-sets used in the Residue number system (RNS) design.

The parallel-prefix tree adders are more favorable in terms of speed and power compare to other adder circuits. Carry generation network is the most important block in parallel prefix tree .The main parallel prefix tree adders are Kogge-Stone, Brent-Kung, and Sklansky parallel prefix adders. Kogge-stone and Brent-Kung adders are mainly used for efficient reverse converter design [6]. Because its offers high efficiency than other parallel prefix structures such as Sklansky parallel prefix adder.

## 2. Related Works

Many works has been carried out in the field of reverse converter design in residue number system. Forward converters are usually classified into two categories based on the moduli used. The first category includes forward converters based on arbitrary moduli-sets. These converters are usually built using look-up tables based converter in RNS. The second category includes forward converters based on special moduli-sets like ($2^n$, $2^n$-1,$2^n$+ 1) is the use of special moduli-sets simplifies the forward conversion process and architectures [4]. ($2^n$, $2^n$-1,$2^n$+ 1) is one of the special moduli-sets used in the Residue number system (RNS) design.

In Piestrak conversion, high-speed realization of a residue-to binary converter for the three-moduli RNS ($2^n$, $2^n$-1,$2^n$+ 1) is based on New CRT [7].It only consists of two stages of full-adders and one 2n-bit 1's complement adder. The full adders are realized by CSA-EAC. The new realization of the converter is based on the CRT. The weighted value of X can be calculated from basic CRT equation computed by using the basic CRT equation. The 3n-bit dynamic range conventional small moduli set is($2^n$, $2^n$-1,$2^n$+ 1). But it is not capable for many applications because of its shorter dynamic range. Another important factor for high speed reverse converter design is the selection of a proper conversion algorithm. Chinese remainder theorem (CRT) based reverse converter have complex computation and complex hardware realization.

In CRT based reverse converter. Conversion formulation can directly mapped to ripple carry adders (RCA),carry save adders, carry propagate adders and carry save adder with end around adders but in conventional adder based reverse converter the conversion delay counteract the speed gain of the residue number system(RNS). The parallel prefix structure in reverse converter helps to achieve high speed operation but it causes increased power consumption in a residue number system.

## 3. Methodology

Reverse converter transforms a residue represented a number into its equivalent weighted number with respect to the corresponding moduli of the moduli-set. But the reverse converter design is more complex than that of the forward converter and modulo arithmetic units in RNS. The Moduli set selection and conversion algorithm are determined the complexity of reverse converter design. The efficient design of reverse converter in residue number systems is used to prevent the slow operation and power consumption in RNS arithmetic operations. The parallel prefix structure helps to achieve faster operation but it causes area overhead and high power consumption in arithmetic operations. So hybrid parallel prefix adder components are used to avoid the area overhead and high power consumption problems in the existing reverse converter design. The 4- moduli sets ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) is used for efficient large dynamic range residue number system (RNS). Reverse converter for the moduli set ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) is based on new Chinese remainder theorems (new CRTs). In the existing adders based reverse converters for moduli set ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) is based on the new CRT for efficient and simple design.

### 3.1 System Overview

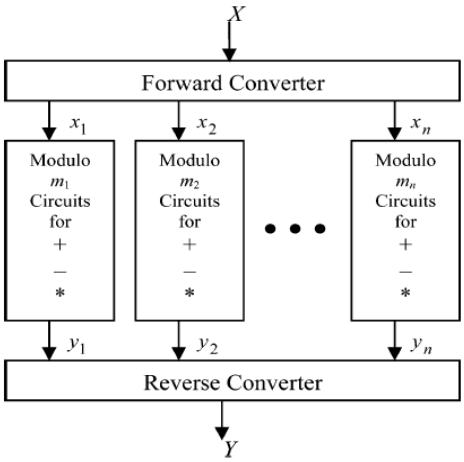


**Figure 1:** Block Diagram of residue number system

The basic block diagram for residue number system (RNS) as shown in the Figure 1. The first step in designing a reverse converter is the moduli set selection. Moduli set selection can play a significant role in dynamic range, speed, and the hardware realization of RNS. The second step for designing a reverse converter is, the values of the moduli of the moduli set must be substituted in new CRT conversion algorithm formulas. Third step, then the resulting equations is simplified by using arithmetic properties and propositions. Finally, final equations are realized by adder components like CSA-EAC, CPA-EAC and CPA. Specific hybrid parallel prefix adder components like hybrid regular parallel prefix XOR/OR(HRPX) adder for (4n+1) bit addition and hybrid modular parallel-prefix excess-one (HMPE) modulus adder for ($2^n$ - 1) modulo addition is used to replace the existing adder components for better power- area trade off in RNS based application.

### 3.2 Reverse converter design

The first step in designing a reverse converter is the moduli set selection. Moduli set selection can play a significant role in dynamic range, speed, and the hardware realization of RNS. The second step for designing a reverse converter is, the values of the moduli of the moduli set must be substituted

in new CRT conversion algorithm formulas. Third step, then the resulting equations is simplified by using arithmetic properties and propositions. Finally, final equations are realized by adder components like CSA-EAC, CPA-EAC and CPA. Specific hybrid parallel prefix adder components like hybrid regular parallel prefix XOR/OR(HRPX) adder for (4n+1) bit addition and hybrid modular parallel-prefix excess-one (HMPE) modulus adder for ($2^n$-1) modulo addition is used to replace the existing adder components .

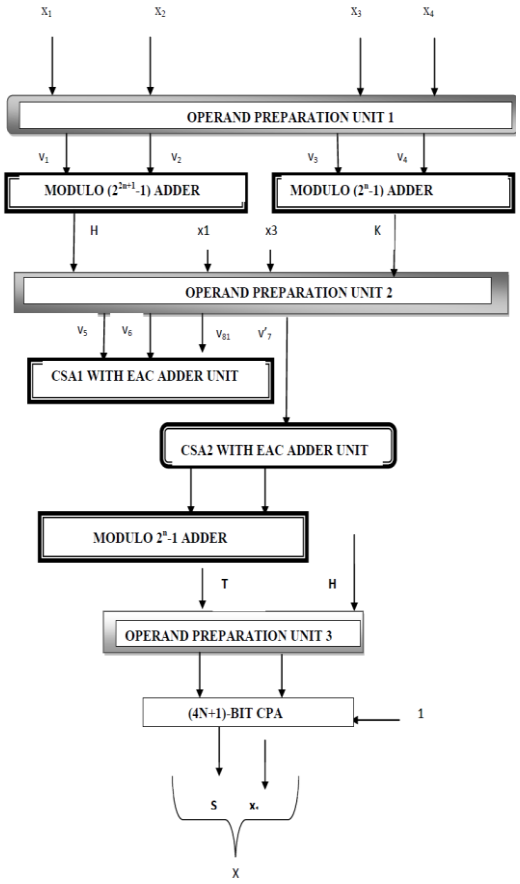


**Figure 3.1:** Converter for moduli set ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1)

The hardware architecture of the adder based reverse converter for the moduli ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) with corresponding residues (x1; x2; x3; x4) is shown figure 3.1. Firstly, the operands preparation unit 1 (OPU) prepares the operands $v_1$,$v_2$,$v_3$ and $v_4$ and the preparations are based on New CRT algorithm for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) These preparations result from the routing of the bits of the residues are based on New CRT algorithm. Operands are

$$v_1 = (x_{2,n-1}\dots x_{2,0})\,(x_{2,2n}\dots x_{2,n+1}\,x_{2,0}) \quad (3.1)$$

$$v_2=(\overline{x_{1,n-1}\dots x_{1,0}})\;\underbrace{1\dots11}_{n+1} \quad (3.2)$$

$$v_3=(x_{4,0}x_{4,n-1}\dots x_{4,0}) \quad (3.3)$$

$$\text{If } v_{3,0}=\begin{cases} v_{41} & \text{if } x_{3,0}=0 \\ v_{42} & \text{if } x_{3,n}=1 \end{cases}$$

$$v_{41}=(x_{3,0}x_{3,n-1}\dots x_{3,1}) \quad (3.4)$$

$$v_{42}=0\,\underbrace{(11\dots1)}_{n-1} \quad (3.5)$$

Modulo ($2^{2n+1}$- 1) addition of v1 and v2 is performed by (2n+1)-bit CPA1 with EAC in existing reverse converter design and H represents the output of modulo ($2^{2n+1}$-1) addition of v1 and v2. Modulo ($2^n$ -1) addition of v3 and v4 are performed by (n) - bit CPA2 with EAC in existing reverse converter design and K represents the output of modulo ($2^n$-1) addition of v1 and v2. Then second operand preparation unit -2(OPU) prepares the operands v5,v6,v81 and v07 and the preparations are based on New CRT algorithm for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) These preparations results from the routing of the bits of x1,x3,and K are based on New CRT algorithm. Operands are

$$H=\left| v_1+v_2 \right|_{2^{2n+1}-1} \quad (3.6)$$

$$K=\left|v_3+v_4\right|_{2^n-1} \quad (3.7)$$

$$v_5=x_{3,n-1}\dots x_{3,0}\,\underbrace{(0\dots00)}_{n-1}\,x_{3,n} \quad (3.8)$$

$$v_6= (K_{n-1}\dots K_0)\,(K_{n-1}\dots K_0) \quad (3.9)$$

$$v_{81}=H_{2n-1}\dots H_1H_0 \quad (3.10)$$

$$v'_7 = x_{1,n-1}\dots x_{1,0}\,\underbrace{1\dots11}_{n-1}\,H_{2n} \quad (3.11)$$

$$T=\left|v_5+v_6+v_{81}+v'_7\right|_{2^n-1} \quad (3.12)$$

Modulo ($2^{2n+1}$-1) addition of v5, v6, v81 and v07 are performed by (2n)-bit CSA1 with EAC, 2n-bit CSA2 with EAC and finally 2n-bit CPA3 with EAC performs the modulo ($2^{2n}$- 1) addition and T represents the output of modulo ($2^{2n}$ - 1) addition and these preparations results from the routing of the bits of T and H. Operands are

$$P= (T_{2n-1}\dots T_0)\,(H_{2n}\dots H_0) \quad (3.13)$$

S=P-T operation is performed by (4n+1)-bit carry propagate adder (CPA) and X (binary number of residues) can be obtained by routing of the bits of X & x1. Here binary number

$$X= (S_{4n}\dots S_1S_0)\,(x_1) \quad (3.14)$$

The simplified resulting equations are realized by carry propagate adder with end around adder (CPA-EAC), CSA with EAC and carry propagate adder. HRPX and HMPE adders are used to delay-power efficient design. HMPE & HRPX adders are used in modified reverse converter design. $2^{2n}$-1 modulo adder is designed by hybrid modular parallel prefix excess-one adder (HMPE). Hybrid regular parallel prefix XOR/OR adder is used for (4n + 1)bit addition to modified reverse converter design. HMPE and HRPX adder components are used to replace the existing adder components like CPA with ECA & CPA in existing reverse converter design.

### 3.3 Hybrid regular parallel prefix XOR/OR adder (BK)

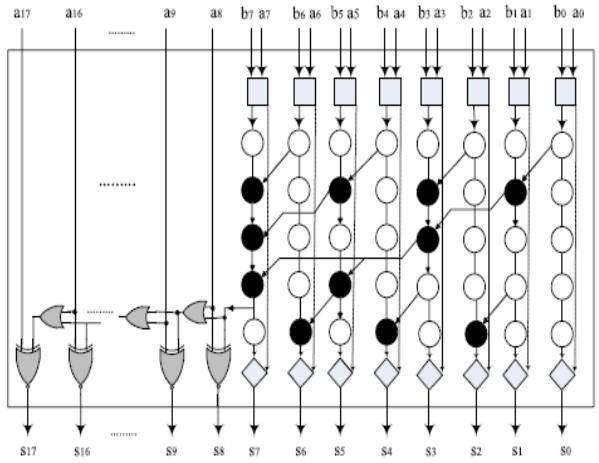


**Figure 3:** Block diagram of HMPE

Hybrid regular parallel prefix XOR/OR adder can perform the subtraction operation in new CRT algorithm formulas derived from 4-moduli set ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1). In HMPX regular parallel prefix adder structure can perform the first part of the addition and the second part of the addition is similar to ripple carry adder logic where the corresponding bits of the operands (P and T) are not constant. Carry chain is not needed in this reverse converter design because residue number system provides a carry free operation. (4n+1) bit CPA (Carry Propagate Adder) for binary subtraction in existing reverse converter design is replaced by Hybrid regular parallel prefix XOR/OR adder.

### 3.4 Modular parallel-prefix Excess one unit

Modulo ($2^n$-1) addition is an important operation in reverse converter design for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) moduli set. The regular CPA with EAC adders are used for modulo ($2^{2n}$-1) addition in existing adder based reverse converter for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) moduli set. Kogge-Stone adder prefix structure is used in HMPE to achieve the high speed with reduced the area cost. Figure 4 shows the Modular parallel prefix excess one unit. Three logic-level basic cells are used for the kogge-stone adder based HMPE and Brent-kung adder based HRPX in the modified high speed reverse converter design.

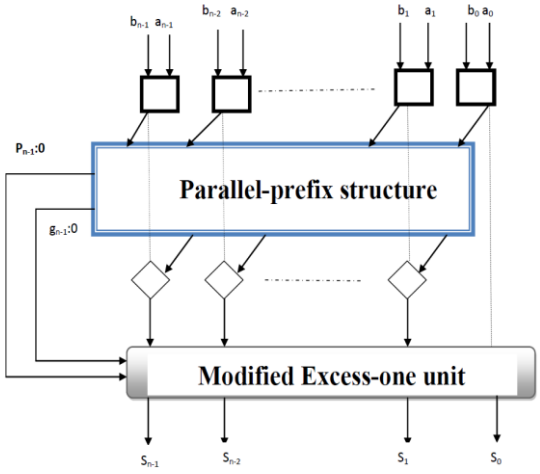


**Figure 4:** Block diagram of HRPX structure

## 4. Results and Discussion

The modules are modeled using VHDL in Xilinx ISE design Suite 13.1 and the simulation of the design is performed using Modelsim SE 6.3f to verify the functionality of the design. Here a structural model of conventional adder based reverse converter with NEW CRT algorithm and Hybrid parallel prefix adders and conventional adders based modified reverse converter with NEW CRT algorithm are developed. Simulation result and synthesis report of the excising and the modified reverse converter are shown below. Figure 5 shows the simulation output of conventional reverse converter based on new CRT for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1). moduli set .where n=4, then the 4 residues are x1,x2,x3 & x4 and inputs are denoted as x1,x2,x3, and x4 . The weighted binary number is obtained from New CRT based algorithm for 4n-bit moduli set. Output will be obtained from residues and is denoted as 'X' in Figure 5

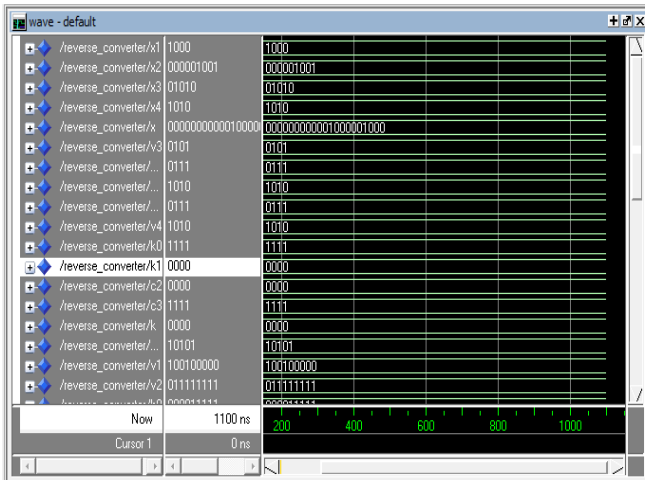


**Figure 5:** Simulation Result of Conventional Reverse Converter Design

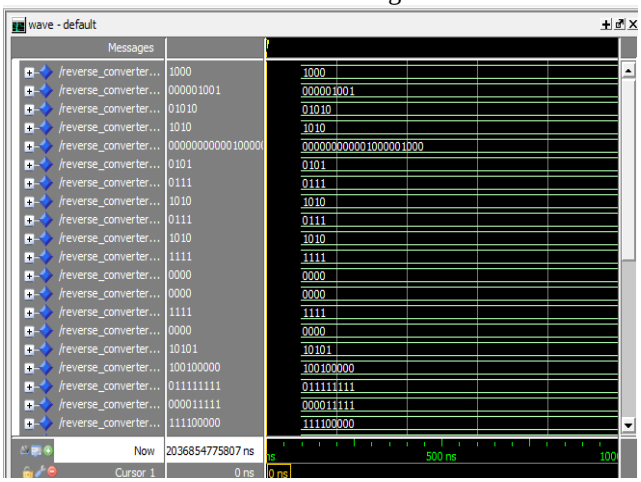


**Figure 6:** Output of conventional Reverse converter based on New CRT for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1).

Figure 6 shows the simulation result of modified reverse converter design. where n=4, then the 4 residues are x1,x2,x3 & x4 and inputs are denoted as x1,x2,x3, and x4 . The weighted binary number is obtained from New CRT based algorithm for 4n-bit moduli set. Output will be obtained from residues and is denoted as 'X' in figure. ($2^{2n}$- 1) modulo addition in reverse converter is performed by HMPE adder

component. (4n+1) addition of reverse converter is performed by HMPX adder components.

**B) Synthesis result of modified and existing reverse converter are shown in Table 1**

**Table 1:** Synthesis results

| | *Conventional reverse converter design* | *Modified reverse converter design* |
|---|---|---|
| Power | 65mW | 62mW |
| Delay | 65ns | 60ns |

Table 1 shows the power utilized by conventional and modified reverse converters design for 4n-bit dynamic range ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1). Moduli set with n=4. The reduction in the power utilization obtained by HMPE & HRPX adders. The power efficiency obtained with the hybrid parallel prefix adder components. From the table it is clear that the modified reverse converter is energy efficient than that of the conventional converters and it is also shows the delay constraints in conventional and modified reverse converters design with n=4. From the table 4.1, it is clear that the modified reverse converter provided high speed gain than that of the conventional reverse converter.

## 5. Conclusion

The modified reverse converter for 4n-bit moduli set with n=4 has been designed, simulated and synthesized. In conventional Reverse converter in residue number systems is more complex and non modular than that of other parts. HMPE & HRPX are applied to the 4-moduli ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) reverse converter architecture to enhance the performance of the reverse converter in terms of delay-power trade off. Kogge -stone adder based HMPE modulo ($2^{2n}$- 1) adder is more area efficient than that of parallel prefix adder based modulo ($2^{2n}$-1) adder. A New CRT algorithm is used for the conversion it leads simple hardware realization. 4-moduli set ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1)) provide better dynamic range and it is sufficient for applications that requires a large dynamic range and more parallelism. Compared to excising adder based reverse converter, the modified converter in my work based on specific hybrid parallel prefix adder components having improved performance in terms of speed and delay. Specific hybrid parallel prefix adder components are used in the reverse converter for increase the speed gain in residue number systems (RNS). The modified reverse converter and forward converter for ($2^n$+1,$2^n$, $2^n$-1, $2^{2n+1}$-1) set in residue number system can be used for filter design applications because of the energy efficient and high speed characteristics of the residue number system.

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