International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Reliable NoC Switch Design with Enhanced Error Handling Capability

Rubina Sabeer[1], Karthika Manilal[2]

[1]P G Scholar, VLSI and Embedded Systems, Department of ECE, T K M Institute of Technology, Kollam, India

[2]Assistant Professor, Department of ECE, T K M Institute of Technology, Kollam, India

Abstract: ***For systems with intensive parallel communication requirements, buses may not provide the required bandwidth, latency, and power consumption. When the number of computational units integrated onto the same silicon die increases, the communication between the PEs become the major issue. A solution for such a communication bottleneck is the use of an embedded switching network, called Network on Chip (NoC), to interconnect the IP modules in SoCs. NoC relies on data packet exchange. But it may causes fault generation or faulty routing of data packets. The existing techniques for routing of data does not have a capacity to accurately locate faulty components in NoC and distinguish both permanent and tolerable errors. Hence a reliable fault tolerant NoC switch called RKT switch based on adaptive routing module proximity algorithm is used to avoid this problem. A loopback module is placed in each port of the router to avoid data loss or trapping of data inside the routers. The frame work could be modified by using convolution encoding and decoding technique so as to improve the systems fault tolerant behaviour. This system can be implemented on FPGA, which offers the advantages such as high performance, fault tolerance. The coding of each module is simulated and synthesized using the Xilinx ISE Design Suite 13.2 and ModelSim Simulator.***

Keywords: SoC, NoC, Loopback, Adaptive XY algorithm, RKT switch, FPGA.

1. Introduction

With the strong advancement in semiconductor processing technologies, the chip integration has reached a stage where a complete system can be placed in a single chip. The whole system - on single silicon leading to the evolution of systems which are known as System on Chip (SoC). Simply a System on Chip (SoC) is an integrated circuit (IC) that integrates all components of an electronic system into a single chip. Applications of these systems are in the area of telecommunications, multimedia, and consumer electronics where it has to satisfy real time requirements.

As technology scales toward deep sub-micron level, the trend of embedded system has been moving towards multiprocessor system-on-chip (MPSoC). It is used by platforms that contain multiple processing elements with specific functionalities reflecting the need of the expected application domain, a memory hierarchy and I/O components. All these components are linked to each other by an on-chip interconnect. Multi-core systems can provide high energy efficiency since they allow the clock frequency and supply voltage to be reduced together to dramatically reduce power dissipation during periods when full rate computation is not needed [2][3].Thus increasing number of computational units will be integrated onto the same silicon die causes tight communication requirements on the communication architecture ie, interconnection between each other becoming a challenging issue. The traditional solution for inter core communication in SoCs such as shared bus systems and point to point links were not able to keep up with the scalability and performance requirements. In most System-on-Chip applications, a shared bus interconnection which needs arbitration logic to serialize several bus access requests, is adopted to communicate with each integrated processing unit because of its low-cost and simple control characteristics. So the integration of network-on-chip (NoC) is done into the SoC.

Network on chip (NOC) is an emerging concept for communications within the large VLSI systems implemented on a single silicon chip[12]. NoC is the communication backbone in a SoC[12]. It provides an effective means to interconnect several processing elements (PEs) or intellectual properties (IPs) (processors, memory controllers, etc.). The NoC mainly consist of both routers and interconnections allowing the communication between the PEs and/or IPs[1]. The router implements the communication protocol. The router basically receives packets from the shared links and according to the address informed in each packet, it forwards the packet to the core attached to it or to another shared link. Network-on-Chip(NoC) provides scalable bandwidth requirement where number of bus requesters is large and their required bandwidth for interconnection is more than the current bus based design. The topology determines how the resources of network are connected, thus, refers to the static arrangement of channels and nodes in an interconnection network. In NOC topology, routing algorithm and switching are main terminology. The routing algorithm is one of the key factor in NOC architecture. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm [7][8].

SoC find their applications mainly in the field of real time systems which works in noisy environments. A real-time application is an application in which execution time must be smaller than a deadline. Otherwise, the computation will be considered as a failure. Thus smaller voltage swings, shrinking feature size etc decreases the noise immunity of the Network on Chips (NoC). Hence, an effective error control scheme is required for ensuring data integrity in Network on chips (NoCs). The two types of error control policies are

switch to switch error controls policy and end to end error control policy. End to end error control policy is the one in which the flits are encoded for error detection/correction in the sender and decoded only at the receiver. One encoder and one decoder are needed to be connected to the network interface, since the sender and receiver is the PE which is connected to the network interface. In the Switch-to-Switch error control policy, the flits are encoded and decoded for error correction/detection in each hop of the transmission from the sender to the receiver. Along with the error correction scheme, the retransmission of erroneous data packets will increases the reliability.

In this work, the main objective is to design and develop a reliable, fault tolerant NoC router called RKT Switch for increasing reliability of data communication through the system.

2. Theory

To meet the growing computation-intensive applications and the needs of low power, high performance systems, the number of computing resources in a single-chip has enormously increased because current VLSI technology can support such an extensive integration of transistors. SoC is the packaging of all the necessary electronic circuits and parts of a system on a single integrated circuit (IC), generally called as a microchip. By adding many computing resources such as CPU, DSP, specific IPs etc to build a system in System-on-Chip, the interconnection between each other becomes a challenging issue. So the integration of network-on-chip (NoC) is done into the SoC. In order to implement a competitive NOC architecture, the router should be efficiently design as it is the central component of NOC architecture. In designing NoC systems, there are several issues to be concerned with, such as topologies, switching techniques, routing algorithms, performance, latency, complexity and so on. An on-chip network is defined mainly by its topology and the protocol implemented by it. Topology concerns the layout and connectivity of the nodes and links on the chip. Protocol dictates how these nodes and links are used[7][8].

The physical topology of a network is the actual geometric layout of workstations. The choice of topology is dependent upon type and number of equipment being used, planned applications and rate of data transfer required, response time and cost. Each topology is suited to specific tasks and has its own advantages and disadvantages. Several network topologies are introduced in NoC designs such as ring topology, mesh topology, torus topology, tree topology etc [7]. When more and more components and switches are incorporated onto a given chip the bandwidth requirement between the computational components will increase but the switching methodology does not have to be changed. Switching techniques define the way and time of connections between input and output ports inside a switch. There exist various switching techniques, but the most popular ones are Circuit Switching, Packet Switching [5] [7].

Second one is Routing Algorithms. A routing algorithm determines a path for a packet to reach its destination. It must be decided within each intermediate router which output channels must be selected for the incoming messages [5][7]. There are various types of routing algorithms differentiated according to their key characteristics. Routing algorithms can be classified as oblivious and adaptive algorithms. Oblivious routing algorithms are the class of routing algorithm which has no information about conditions of the network, like traffic amounts or congestion. A router makes routing decisions on the grounds of some algorithm[7]. Adaptive routing algorithms do not restrict a message to a single path when traveling from the source to the destination. While making a decision the current network conditions are considered. This makes the routing more flexible and reduces unnecessary waiting time delays, providing better fault tolerance [7].

The third one is Routing Modes .Network flow control, also called as routing mode, determines how packets are transmitted inside a network. Different types of flow control mechanism are store and forward flow control, virtual cut through flow control and wormhole flow control.In Store-and-Forward switching, it will wait until the entire frame has arrived prior to forwarding it. This method stores the entire frame in memory. Once the frame is in memory, the switch checks the destination address, source address, and the CRC. If no errors are present, the frame is forwarded to the appropriate port. This process ensures that the destination network is not affected by corrupted or truncated frames [7]. In Cut-Through switching, it will begin forwarding the frame as soon as the destination address is identified. The difference between this and Store-and- Forward is that Store-and-Forward receives the whole frame before forwarding. Since frame errors cannot be detected by reading only the destination address, Cut-Through may impact network performance by forwarding corrupted or truncated frames [7]. These bad frames can create broadcast storms wherein several devices on the network respond to the corrupted frames simultaneously. In Wormhole Switching, the message is divided into flits. This is done in order to decrease the buffer size at routers and to achieve much faster routers. A message is sent through the network at it level in pipelined fashion. The header flit contains the routing information and builds a path in the network, which the other its follow. When a message is blocked it occupies several routers in the path constructed so far and a few flits needs to be buffered at a router. As a result there is no need for a local processor memory to buffer messages, which significantly reduces average message latency. However, only the header flit contains the routing information and each incoming data it is simply forwarded along the same output channel as the preceding data flit, which requires that the message must cross the channel in its entirety before it can be used by another message [7].

3. Methodology

Network on Chip provides the infrastructure for the communication in multicore single chip systems. A NoC consists of resources and switches that are connected using

channels so that they are able to communicate with each other by sending messages. Here the topology used is mesh, which is a simplest layout and local connectivity, also routing in a two-dimensional mesh is easy so it can make small switches, which have high capacity, short clock cycle, and overall scalability. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm. Many routing algorithms are introduced in NoC designs.

3.1 RKT switch

The RKT switch based NoC is a reliable communication approach. This is a packet switched network. The architecture is shown in figure 1. Its architecture consist of four ports such as north, south, east and west and it is suitable for a 2D-mesh NoC. The 2D mesh model allows the placement of components anywhere on the network. The processing elements or IPs can be connected to any side of the router. In this, an IP can replace many routers by having several input ports. Hence it can be strongly connected in the network. This reliable RKT switch can also be suitable for NoC having five ports (East, South, North, West and Local port). In each direction, the port consist of two unidirectional data buses ie, input port and output port. Each input port is composed of buffer and routing logic block.

The operation of RKT switch is based on store and forward switching technique. Wormhole routing is an ideal candidate switching technique for on-chip multiprocessor interconnects networks because this mode requires less

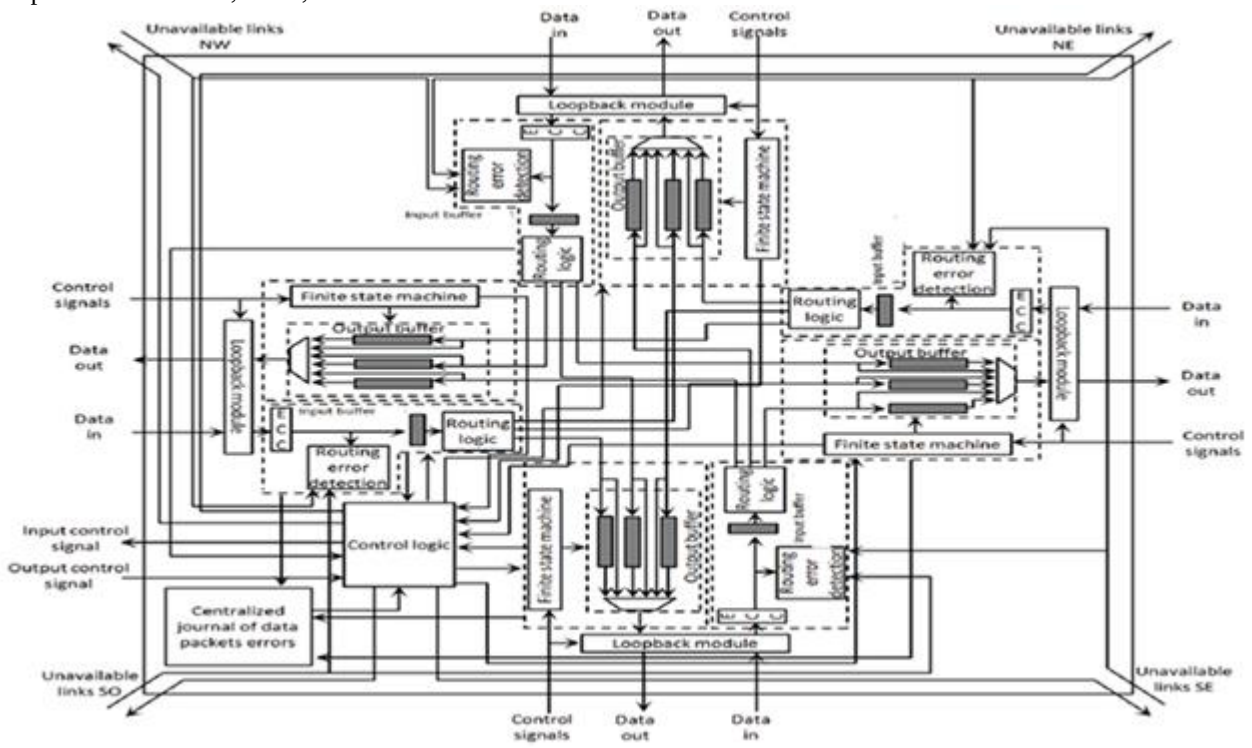

Figure 1: Architecture of RKT Switch

memory than the two other modes since only one flit has to be stored at once and also it reduces the store and forward delay. But for a dynamically reconfigurable NoC, store and forward technique is suitable. In store and forward technique, it will wait until the entire frame has arrived prior to forwarding it ie, each data packet is stored only in a single router where as in wormhole routing technique, a single packet is divided into small and equal sized flits. So the time required to clear all the routers containing flits and to reconstructing these packets before performing reconfiguration is significant.

3.2 Loopback Module

During dynamic reconfiguration, the position and the number of components in network can be change and due to this there is a chance for fault occurance. Whenever a new component is placed on the network, it covers the routers in its area. Thus, the data packets cannot be sent inside the area being reconfigured. These regions become dynamically isolated and leads to data packet losses or increase packet transmission latency. Thereby, these data packets remain stored in the output routers until the end of the reconfiguration during dynamic implementation or are lost in the case of detection of a permanent faulty node. To overcome these drawbacks, the RKT-switch contains an output buffer blocks associated with loopback modules.

This loopback module emptying the buffers of each output port by looping back the data packets to input port of the router. So the data packets cannot trapped inside the buffer when a neighboring switch is detected as permanently faulty. Thus reduces latency when a neighbor has suffered a dynamic reconfiguration. These loopback modules are implemented in each of the four ports of the RKT switch as shown in figure. 1.

The architecture of the loopback module is depicted in figure.2.

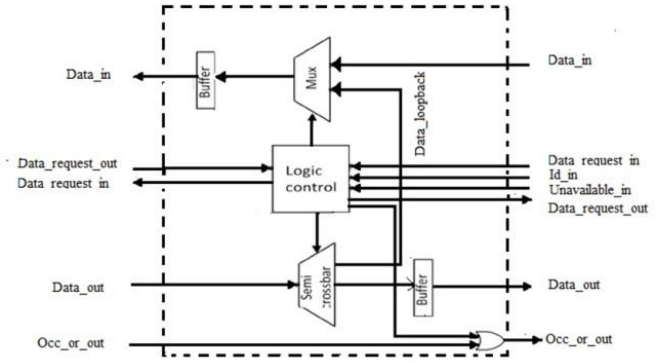

Figure 2: Architecture of Loopback Module

It consist of a logic control block, mux, buffers and a semi crossbar switch which act as a demux. The logic control block checks the availability of the neighboring router in order to transmit the data packets (data request in signal). If no loopback is required, a semicrossbar connects the buffer to the data out signal in order to send the data packets towards the neighboring router and activates the data request out signal. Next, a multiplexor connects the input data bus to the data in bus. When a loopback is required, due to the unavailability of a neighboring router or permanent error detection, the logic control block configures the semi crossbar block to send the considered data packet on the data loopback bus. Therefore, the data packet is looped back inside the router and will be considered as a new packet. During this, in order to avoid the reception of a new data packet from the neighboring switch, the occ out signal is activated.

3.3 Routing Error Detection and Routing Logic

A routing error detection block is present in each port of a RKT switch. It checks the availability of each port and set Unique Routing Path Indication (URPI) bits. URPI bits set when a router has only one port is available for transmission and otherwise it to be 00. This bits are placed on the 15th and 16th position of data packet. Also this block assign the data transmission direction and transmit data to output. Thus, this bits allows the avoidance of false detections.

Table 1: Structure of Data Packets

URPI bits (16-15)	Y previous	X previous	Y destn	X destn	Data

There is a routing logic block present inside the each port of the router which switches the data from the input port of a particular direction of router to the output port of the desired location by the adaptive XY routing algorithm. According to this, it compare the coordinates stored in header flit with the previous address coordinates and thus finds out the direction to which the packet has to be switched. If the value in Y coordinate of header is greater than the previous Y coordinate value then request signal goes to east port otherwise to west port. If both value are equal then X coordinate is compared, if X coordinate of header is greater than that of previous value, then request signal goes to south port otherwise to north port.

Table 2: Routing Logic

Conditions	*Direction*
Y destination > Y previous	East
Y destination < Y previous	West
Y destination = Y previous X destination > X previous	South
X destination < X previous	North

3.3 Convolution Encoding and Decoding

Convolutional codes are used extensively in numerous applications in order to achieve reliable data transfer. Convolution encoding is a Forward Error Correction technique used in continuous one-way and real time communication links. Data errors can be detected using this technique. Convolution encoding is accomplished using a shift register and associated combinatorial logic that performs modulo-two addition. This encoded datas are decoded by using the trellis to find the most likely sequence of codes. The Viterbi algorithm simplifies the decoding task by limiting the number of sequences examined. The most likely path to each state is retained for each new symbol. By this, more number of errors can be detected and corrected.

4. Results and Discussion

The modules are modelled using VHDL in Xilinx ISE Design Suite 13.2 and the simulation of the design is performed using ModelSim SE 5.7F to verify the functionality of the design. Here a structural model of router is developed. The Network on chip router contains modules such as FIFO buffers, XY routing logic, FSM, Loopback modules, Routing error detection modules, Routing Logic, NoC router etc.

4.1 Simulation of Buffer

Buffer is actually a data structure which is used for temporarily storing the data inside router before switching it to desired direction. The status of FIFO decides whether the communication can start or not. If the FIFO is empty the data can be written in it and communication can start .If FIFO is full, data can be read or can be forwarded to its destination router. A buffer module consist of input signals such as clock, read, write, data input and output signals such as empty buffer, full buffer and data output. Read and write are the control signals which enable the read and write operations in FIFO buffer. Data input is the input which has to be stored in the buffer and data output will be the output data read from the buffer. In this design, the signal r and w corresponds to read and write signals, d and q are the input and output data of buffer respectively, buffer full and buffer empty signals shows the status of the buffer.

4.2 Simulation of FSM

FSM controls the read and write operation of FIFO according to its status. If FIFO is empty and having space to store the data, FSM will generate acknowledgement signal in respect to the request coming to the input channel, thus write operation starts. If FIFO is full or not having space to store the data, the write operation stops. When the FIFO is full, FSM will send request to output channel of other port, if

grant signal is received by it then read operation starts. It consist of three states such as transmit, receive and loopback.

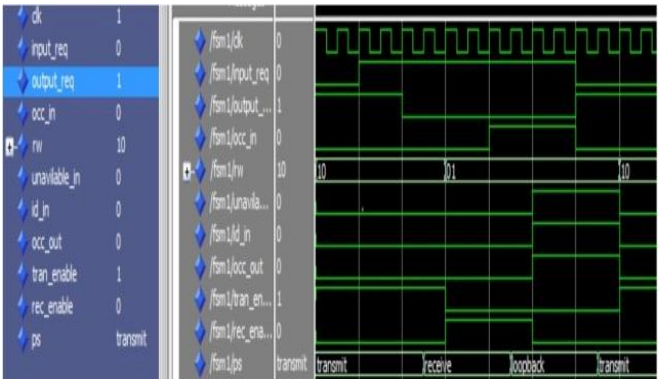

Figure 3: Simulation of FSM

4.3 Simulation of Routing error detection.

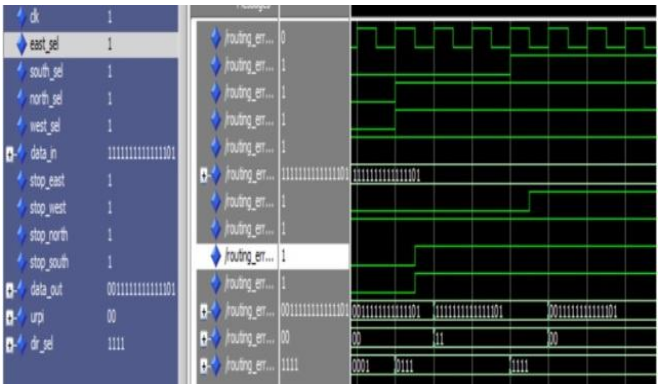

Figure 4: Simulation of Routing Error Detection

Routing error detection module in RKT switch checks the availability of each port and set Unique Routing Path Indication (URPI) bits added to the header of the data packets. This bits avoids the false detections and prevent the faulty routing decision. URPI bits sets only when one port is available for transmission. Otherwise this become ”00”. Also this assign direction of data transmission and transmit data to corresponding output port. After appending the URPI bits, this block send data to the routing logic module.

4.3 Simulation of Loopback Module

When a permanent fault is detected or neighboring node become unavailable and the data become trapped inside the output buffers of each router until the end of operations. Then the loopback module reroute the data and the router adds ”1” to error journal associated with the faulty routing logic block. Data in, Data out, occ out, Data req in, Data req out ,id in and unavailable in are given as inputs and occ or out is taken as output signal. If occ or out signal is activated, it indicate that the data packet is looped back inside the router and avoid the reception of a new packet from neighboring node. Otherwise normal operation is carried out.

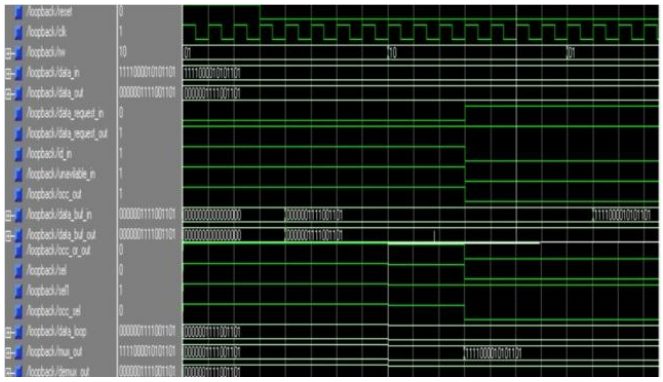

Figure 5: Simulation of Loopback Module

4.4 Simulation of Routing Logic

It first check the URPI bits and adaptive XY algorithms is used when more output ports are available at the same time. According to adaptive XY algorithm, it compare the coordinates stored in header flit with the previous address coordinates and thus finds out the direction to which the packet has to be switched.

Figure 6: Simulation of Routing Logic

4.5 Simulation of North and West Modules

During normal operation, the input given at west port is received at the north port and Vice versa. Otherwise the data packet is looped back. Then the data is considered as a new packet and occ_or_out signal indicate as “1”.

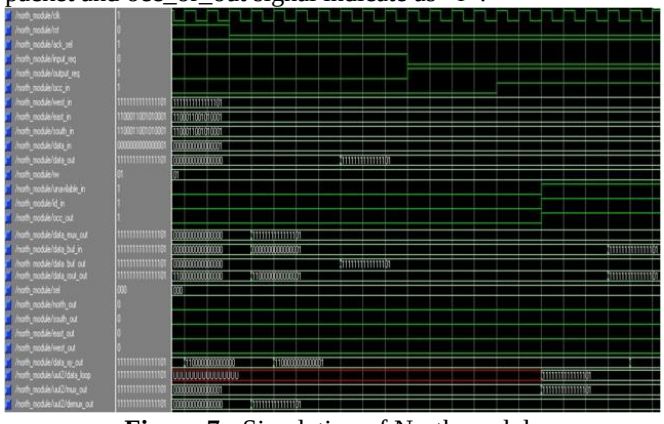

Figure 7: Simulation of North module

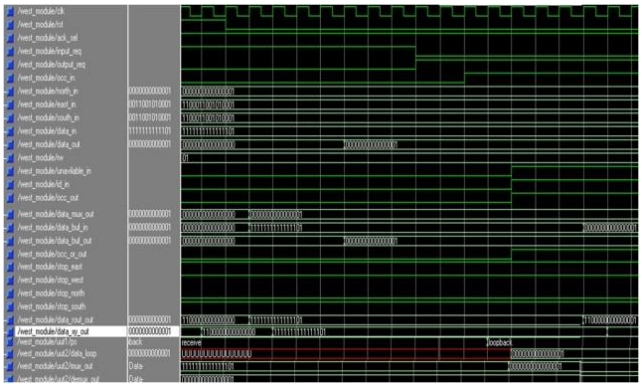

Figure 8: Simulation of West Module

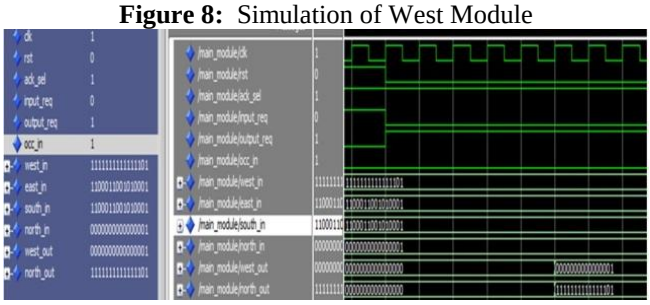

Figure 9: Simulation of NoC Router

5. Conclusion

This work intends to develop a reliable dynamically reconfigurable NoC switch called RKT switch. NoCs consist of routers and interconnections. The path for a data packet between source and destination is defined by a routing algorithm. Commonly, adaptive routing algorithms are used. But it may causes fault generation or faulty routing of data packets. For a fault tolerant NOC design, many routing algorithms such as XY routing algorithm, turn model, adaptive turn model etc have been used. But these methods does not have a capacity to accurately locate faulty components in NoC and distinguish permanent and tolerable errors. So a reliable fault tolerant reliable NoC switch called RKT switch based on adaptive routing module proximity algorithm is used. It is based on both XY algorithm and adaptive turn model. Here the routing decision is taken by the router according to the XY routing logic present in router module. If any data packet become trapped inside the output buffers, lead to a fault routing decision, a loopback module is placed in each port of the router to empties the buffer. By using Convolution encoding and decoding more number of errors can be detected and corrected. Thus, this fault tolerant reliable Noc provides better results This work is synthesized in Xilinx ISE design suite 13.2 and simulated in ModelSim SE 6.3f.

References

[1] Cedric. Killian, Camel Tanougast, Fabrice Monteiro, and Abbas Dandache , “Smart Reliable Network-on-Chip”, IEEE Transactions on Very Large Scale Integration Systems, VOL. 22,NO.2, February 2014.

[2] Mr. N. Subhananthan , Mrs. C. G. Joy Merline M.E, “Efficient And Advance Routing Logic For Network On Chip”, Internatioal Journal of Engineering Research and Applications (IJERA), International Conference on Humming Bird, March 2014.

[3] Rohini, Dr.G.R.Udupi, G.A.Bidkar , “Design and implementation of deadlock free NoC Router Architecture ”, International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE),Vol.2,April 2013.

[4] Ms. P.B. Domkondwar, “Router Architecture for Network on Chip Using FPGA ”, International Journal of Scientific & Engineering Research ,Volume 3, Issue 5, May-2012.

[5] Shubhangi D Chawade, Mahendra A Gaikwad, Rajendra M Patrikar, “ Review of XY Routing Algorithm for Network-on-Chip Architecture ”, International Journal of Computer Applications, April 2012.

[6] Ms. A.S. Kale, M.A.Gaikwad , “ Design and Analysis of On-Chip Router for Network On Chip ”, International Journal of Computer Trends and Technology, July to Aug Issue 2011.

[7] Zaheer Ahmed ,” Fault Adaptive Routing ”, Institute fr Technische Informatik, Universitt Stuttgart, June-2009.

[8] Maksat Atagoziyev , “ Routing Algorithms for On Chip Networks ”, Middle East Technical University,December 2007.

[9] JieWu , “ A Fault-Tolerant and Deadlock-Free Routing Protocol in 2D Meshes Based on Odd-Even Turn Model ”, IEEE Transactions On Computers, Vol. 52,Sept 2003.

[10] G.-M. Chiu , “ The odd-even turn model for adaptive routing ”, IEEE Trans. Parallel Distrib. Systems, Jul. 2000.

[11] P. Lysaght and J. Dunlop ,” Dynamic reconfiguration of FPGAs ”, in Proc. Int. Workshop Field Program. Logic Appl. More FPGAs. 1994.

[12] Swati Malviya, Anurag Jaiswal ,” Five Port Router for Network on Chip ”, Capgemini Consulting India Pvt.Ltd.

[13] Dr. Preeti Bajaj, Dinesh Padole ,” Arbitration Schemes for Multiprocessor Shared Bus ”, New Trends and Developments in Automotive System Engineering.

[14] Christophe Bobda, Ali Ahmadinia ,” Dynamic Interconnection of Reconfigurable Modules on Reconfigurable Devices ”, IEEE CS and the IEEE CASS.