International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Comparative Analysis of Adders

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Abstract: ***In digital circuits, an adder is the most common block used to perform addition of numbers or bits. Adder can be implemented as half adder or full adder, depending on the requirement. In this paper, one bit static full adder schematic is generated (along with it's layout using tool Mentor Graphics Hep 1) and is simulated for transient analysis and then this as component is used to implement different types of four bit adders like Ripple carry adder, Carry select adder, By pass adder and Carry look ahead adder. Transient analysis for the same is done along with comparison of these adders based on parameters like: power dissipation, delay, no. of gates and average no. of logic transitions and finally the conclusion is drawn.***

Keywords: Ripple carry adder, Carry select adder, By pass adder, Carry look ahead adder, Power dissipation, Delay, No. of gates.

1. Introduction

Adder can be implemented as Half adder or Full adder. In Half adder, it adds two binary bits *A* and *B* at a time and generates two outputs, Sum (*A* XOR *B*) and Carry (*A* AND *B*) (where XOR and AND are logic gates). In Full adder, it adds three binary bits at a time, *A*, *B*, and C_{in} where *A* and *B* are the bits to be added, and C_{in} is a bit carried in from the next less significant stage and generates Sum (*A* XOR *B* XOR C_{in}) and Carry ((*A* AND *B*) OR (C_{in} AND (*A* OR *B*))) at output. Fig. 1 shows one bit static full adder with inputs as *A*, *B* and C_i and output Sum (*S*) and Carry (C_o) [1].

1.1 Adder Types

There are different types of full adders like one, listed below:

1. Ripple carry adder: N-bit Ripple carry adder is formed by placing N Full adder in series. However computing final carry takes lot of time. This means lot of delay occurs in propagating carry and it increases with increase in size of N (Refer Fig. 2) [1]-[4].
2. Carry select adder: Here 2 sets of ripple carry adder are used, for 1 set of input, C_{in} =0 and for other set C_{in} = 1 is kept. Hence the carry is already calculated and through MUX the sum bits are selected and final carry is founded using both sets of adder and hence time taken to compute carry reduces. This circuit is however faster than ripple carry adder but it occupies large area and has high power dissipation as compared to ripple carry adder [1]-[4].
3. Carry look ahead adder: The carry for each stage is calculated in advance and hence total delay is significantly reduced. Therefore the final carry is quickly computed in this case. Here S_i and C_i at each stage (where '*i*' is any stage) is computed at same time, hence it is the fastest adder (Refer Eqn. 1 to 4) (Refer Fig. 3) [1]-[4].

$$G_i = A_i \cdot B_i \quad (1)$$

$$P_i = A_i \oplus B_i \quad (2)$$

$$C_i = G_i + (P_i \cdot C_i) \quad (3)$$

$$S_i = P_i \oplus C_i \quad (4)$$

4. Carry by pass adder: This is another way to reduce delay in computing final carry (Refer Fig. 4) (Refer Eqn. 1, 2, 4 and 5 (Where ByPassLogic =1 when P_0=P_1=P_2=P_3=1, else it is =0) [1]-[4].

$$C_{03} = ((G_3 + P_3 \cdot C_3) \cdot \overline{ByPassLogic}) + (C_{i0} \cdot ByPassLogic) \quad (5)$$

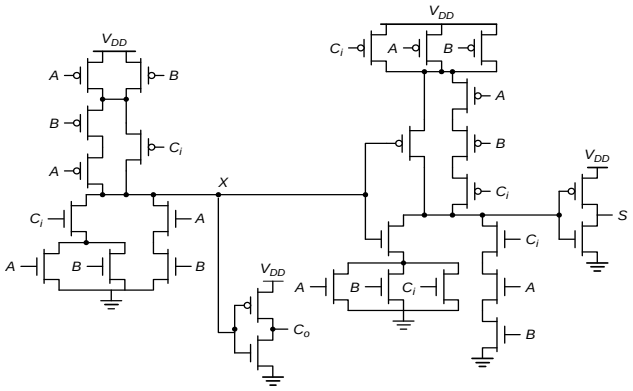

Figure 1: One bit static full adder [1]

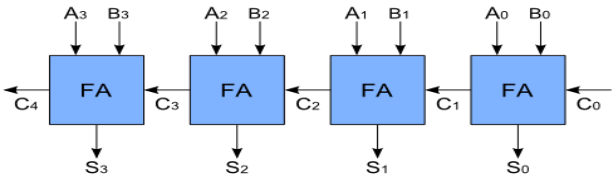

Figure 2: 4 bit Ripple carry adder [1]

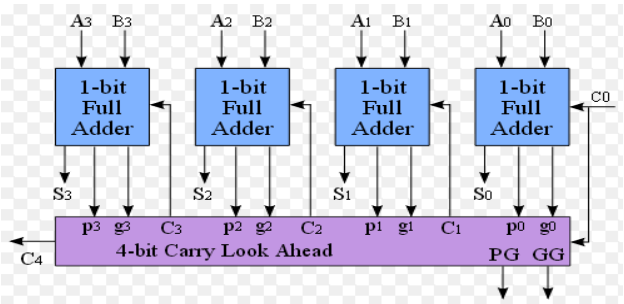

Figure 3: 4 bit Carry look ahead adder [1]

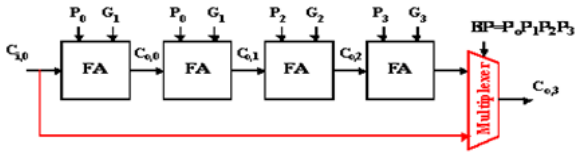

Figure 4: 4 bit Carry by pass adder [2]

2. Experimental Set up and Results

This section is split into five subsections (2.1 to 2.5), where schematic diagrams and transient analysis is discussed [5-13].

2.1 One bit Static Adder

The schematic of one bit static full adder is generated (Refer Fig. 5 for test bench and Fig. 6 [2] for schematic, which is same as Fig. 1) and the transient analysis is done (Refer Fig. 7) and then layout is generated (Refer Fig. 8) and then parasitic capacitance is extracted, so Pex report (Refer Fig. 9) and post layout simulation waves (Refer Fig. 10) are also shown. The power dissipation and delay analysis is done in Table 1 and 2 respectively.

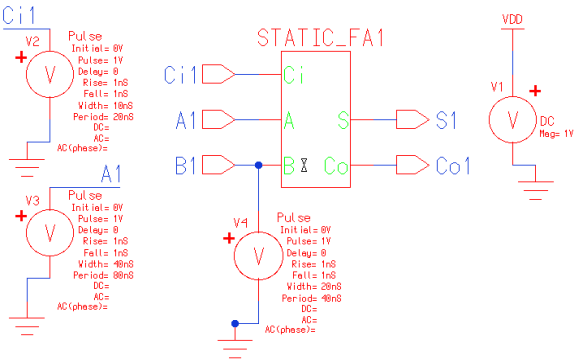

Figure 5: Testbench for one bit adder

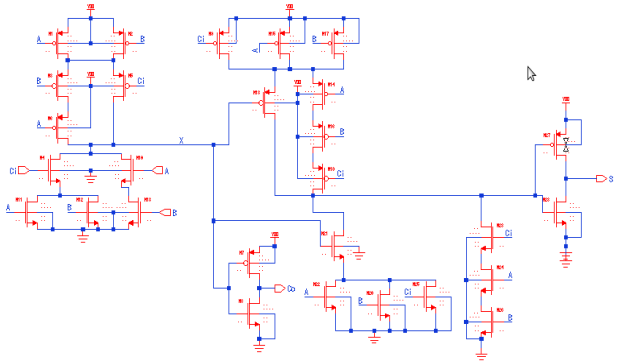

Figure 6: Schematic of static one bit full adder

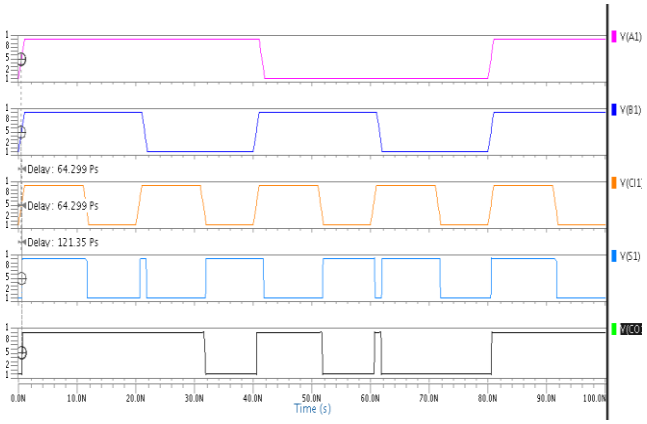

Figure 7: Simulation waves

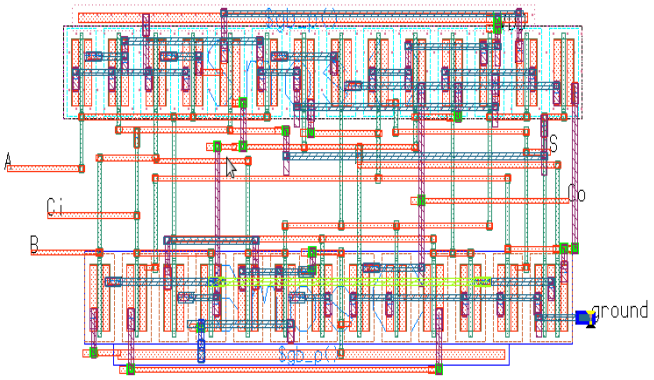

Figure 8: Layout of Schematic (one bit adder)

No.	Layout Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	VDD	59	9.24970E-12	9.88886E-14	9.34859E-12
2	ground	98	1.15163E-11	5.78957E-14	1.15742E-11
3	3	35	4.23355E-12	3.86813E-14	4.27223E-12
4	4	22	3.72808E-12	1.20640E-14	3.74014E-12
5	5	66	9.59324E-12	5.97982E-14	9.65304E-12
6	6	18	1.79924E-12	3.47292E-14	1.83397E-12
7	7	76	1.09652E-11	9.69531E-14	1.10621E-11
8	8	32	3.09001E-12	2.18400E-14	3.11185E-12
9	Co	22	3.36475E-12	5.12460E-14	3.41600E-12
10	10	12	9.10584E-13	1.01322E-14	9.20716E-13
11	S	31	3.53052E-12	3.37048E-14	3.56422E-12
12	12	48	5.47311E-12	6.30325E-14	5.53614E-12
13	13	41	4.29764E-12	6.25245E-14	4.36016E-12
14	14	16	1.49577E-12	5.51200E-15	1.50129E-12
15	15	16	2.23045E-12	4.00655E-14	2.27051E-12
16	16	13	1.57039E-12	2.00530E-14	1.59044E-12
17	A	58	1.16821E-11	7.88803E-14	1.17610E-11
18	B	63	1.23381E-11	6.87272E-14	1.24069E-11
19	Ci	54	1.05230E-11	5.89084E-14	1.05819E-11

Figure 9: Parasitic Capacitance

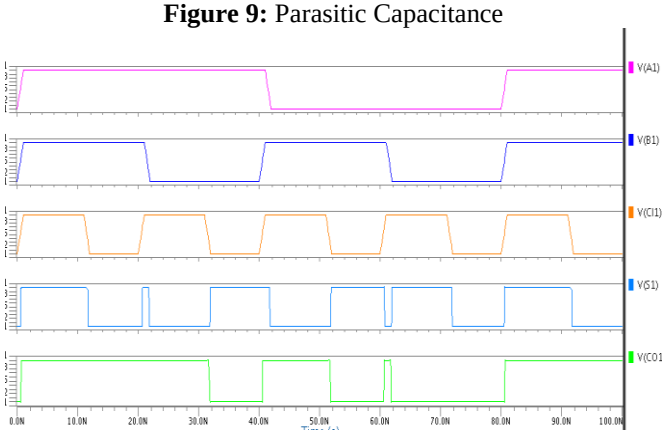

Figure 10: Post layout Simulation waves

Table 1: Voltage v/s Power dissipation

Operating Voltage (V)	Power Dissipation Recorded (N Watt)
0.6	1.5415
0.8	2.3149
1	3.2388
1.2	4.3364
1.4	5.6359

Table 2: Delay Analysis

Input Signal	Output Signal	Delay Recorded
A1, B1	CO1	121 ps
A1, B1	S1	64.299 ps

2.2 Ripple Carry Adder

Schematic of Ripple carry adder (RCA) is generated using one bit adder as component, same as Fig. 2 (Refer Fig. 11 for test bench and symbol [2]). Upon transient analysis, waves are generated (Refer Fig. 12). Table 3 and 4 shows power dissipation and delay analysis respectively.

Table 3: Voltage v/s Power (RCA)

Operating Voltage (V)	Power Dissipation Recorded (N Watt)
0.6	5.078
0.8	7.8716
1	11.3610
1.2	15.6848
1.4	21.0160

Table 4: Delay analysis (RCA)

Input Signal	Output Signal	Delay Recorded
A1	S1	600.45 ps
A1	S2	723.87 ps
A1	S3	931.59 ps
A1	S4	931.59 ps
A1	CO1	19.637 ns

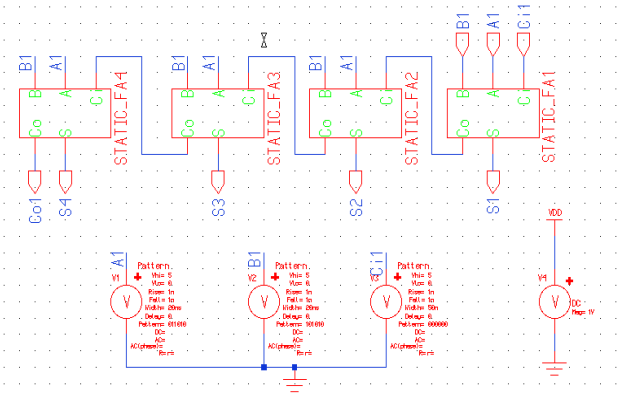

Figure 11: Testbench for Ripple carry adder

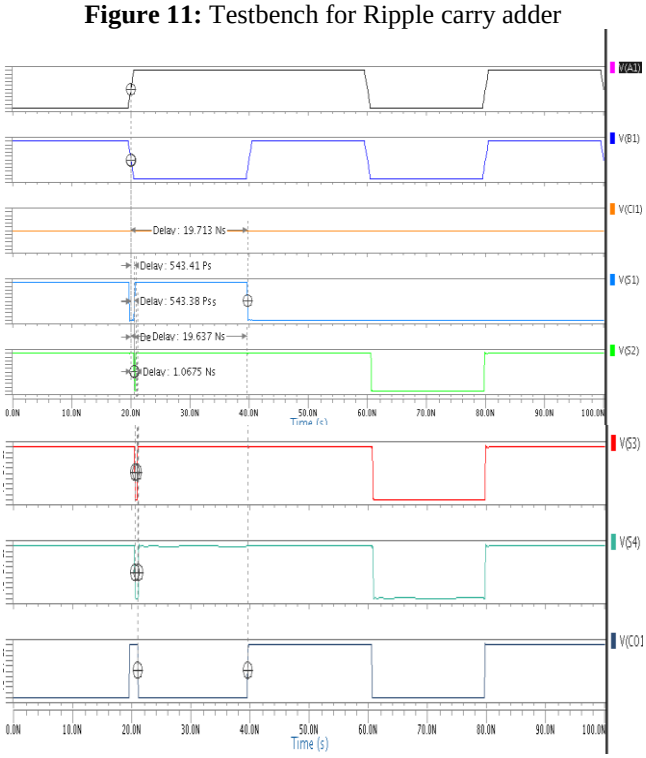

Figure 12: Simulation waves for Ripple carry adder

2.3 Carry Select Adder

Schematic of Carry select adder (CSA) [2-3] is generated (Refer Fig. 13) where the main block 'Carry select adder' is described in Fig. 14 which again contains blocks like static full adder (Fig. 6), MUX, AND gate and OR gate (Refer Fig. 15-17). Upon transient analysis, waves are generated (Refer Fig. 18). Table 5 and 6 shows power dissipation and delay analysis respectively.

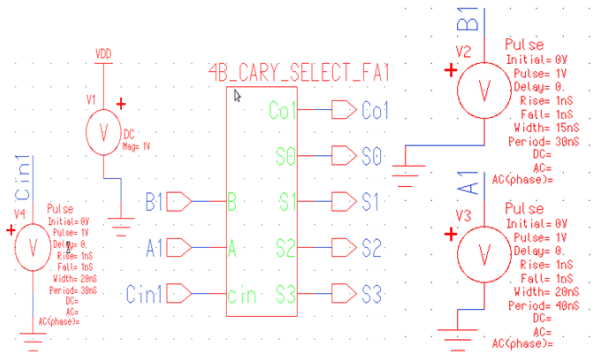

Figure 13: Testbench for Carry select adder

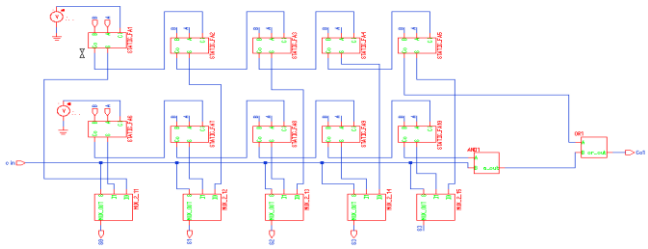

Figure 14: Schematic of Carry select adder

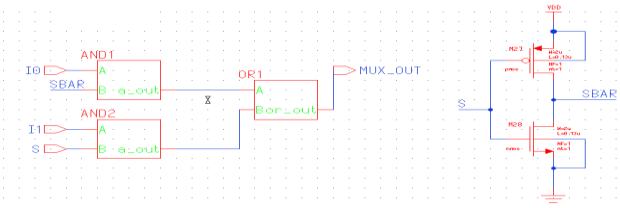

Figure 15: Schematic of MUX

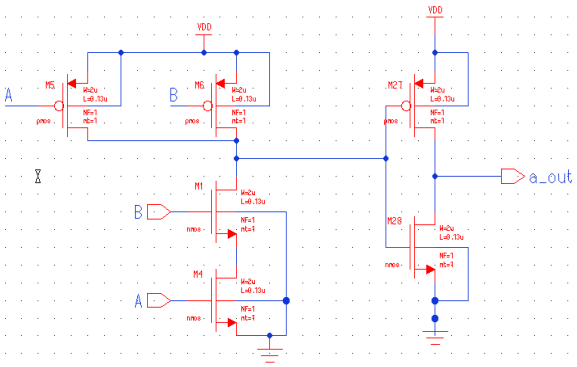

Figure 16: Schematic of AND gate

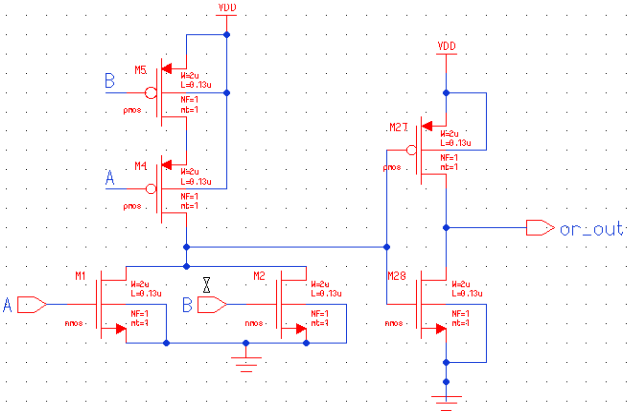

Figure 17: Schematic of OR gate

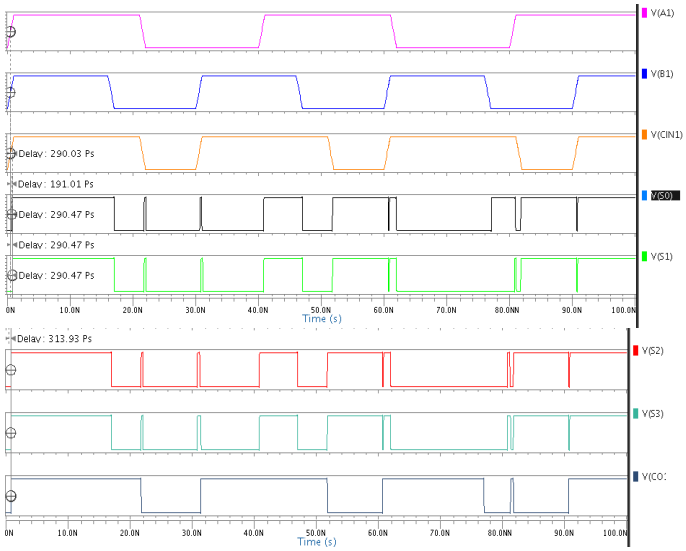

Figure 18: Transient waves for Carry select adder

Table 5: Voltage v/s Power dissipation (CSA)

Operating Voltage (V)	*Power Dissipation Recorded*
0.6	23.579 N Watt
0.8	35.7119N Watt
1	50.4988 N Watt
1.2	183.8536 N Watt
1.4	7.8590 U Watt

Table 6: Delay analysis (CSA)

Input Signal	*Output Signal*	*Delay Recorded*
A1	S0	191.01 ps
A1	S1	290.03 ps
A1	S2	290.47 ps
A1	S3	290.47 ps
A1	CO1	313.93 ps

2.4 Carry Look Ahead Adder

Schematic of Carry look ahead adder (CLA) is generated [2-3] (Refer Fig. 19 for test bench and Fig. 20 for symbol which again contains blocks like Partial full adder, XOR gates, AND gate, OR gate etc (Refer Fig. 21-22)). Upon transient analysis, waves are generated (Refer Fig. 23). Table 7 and 8 shows power dissipation and delay analysis respectively.

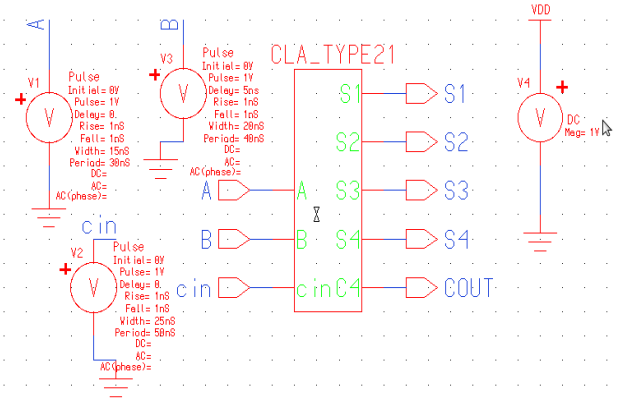

Figure 19: Testbench for Carry look ahead adder

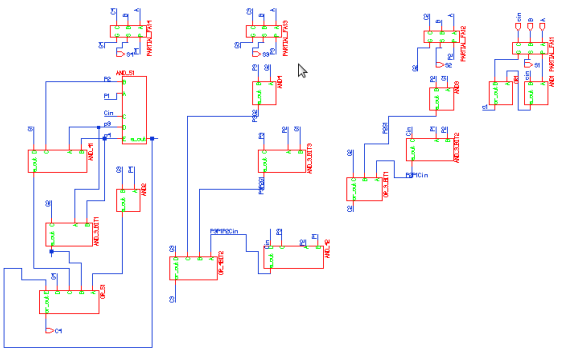

Figure 20: Schematic of Carry look ahead adder

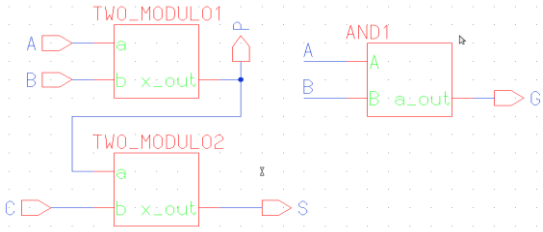

Figure 21: Schematic of Partial ful adder

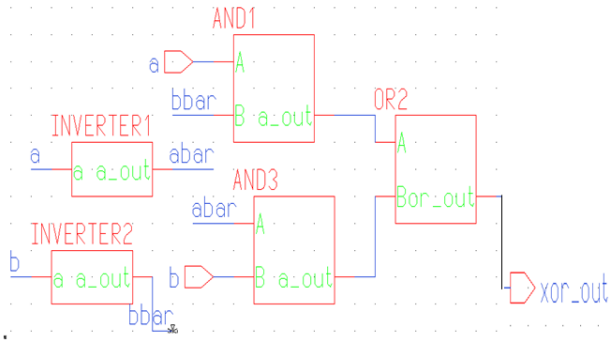

Figure 22: Schematic of XOR gate (Two_Modul)

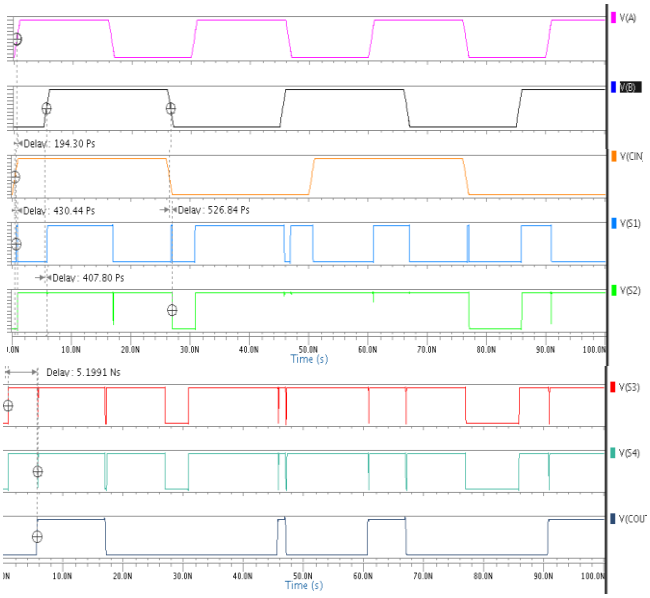

Figure 23 : Transient waves (CLA)

Table 7: Voltage v/s Power dissipation (CLA)

Operating Voltage(V)	*Power Dissipation Recorded (N Watt)*
0.6	18.7358
0.8	28.8346
1	41.340

1.2	56.7134
1.4	75.5243

Table 8: Delay analysis (CLA)

Input Signal	*Output Signal*	*Delay Recorded*
A	S1	194.30 ps
A	S2	194.30 ps
A	S3	194.30 ps
A	S4	194.30 ps
A	COUT	194.30ps

2.5 Carry By Pass Adder

Schematic of Carry by pass adder (CBA) is generated, same as Fig. 4 (Refer Fig. 24-25 for test bench and symbol respectively). Fig. 25 contains blocks like Partial full adder, MUX, AND gate, static full adder (Fig. 6). Upon transient analysis, waves are generated (Refer Fig. 26). Table 9 and 10 shows power dissipation and delay analysis respectively.

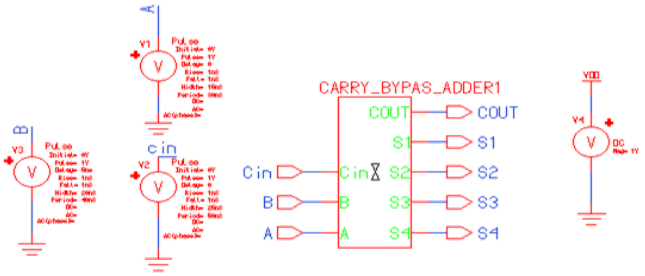

Figure 24: Testbench for Carry by pass adder

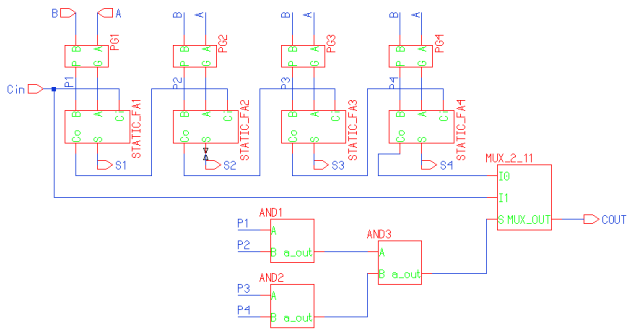

Figure 25: Schematic of Carry bypass adder

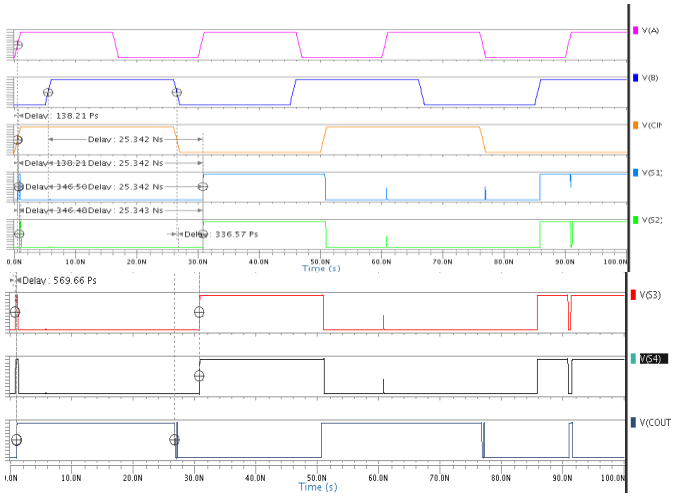

Figure 26: Transient waves for Carry bypass adder

Table 9: Voltage v/s Power dissipation (CBA)

Operating Voltage (V)	*Power Dissipation Recorded (N Watt)*
0.6	16.1188
0.8	24.5099
1	34.7288
1.2	47.0961
1.4	62.0084

Table 10: Delay analysis (CBA)

Input Signal	Output Signal	Delay Recorded
A	S1	138.21 ps
A	S2	336.57 ps
A	S3	336.57 ps
A	S4	336.57 ps
A	COUT	569.66ps

3. Conclusion

After analysis, it can be concluded that power dissipation increases with increasing voltage, and also power dissipation is a function of input vector. Power dissipation is maximum for carry select adder and is least for Ripple carry adder. Delay is more in Ripple carry adder and is least in Carry look ahead adder. No. of gates is least in Ripple carry adder and highest in carry select adder. Average no. of logic transitions is more in carry select adder and least in Ripple carry adder.

References

[1] http://en.wikipedia.org/wiki/Adder_%28electronics%29
[2] A.P. Chandrakasan, Samuel Sheng, and Robert W. Brodersen, "Low-power CMOS digital design," IEEE Journal of Solid-State Circuits, vol. 27, pp. 473-484, 1992.
[3] J. M. Rabaey and M. Pedram, Low Power Design Methodologies, Norwell: Kluwer Academic Publishers, pp. 161-186, 1996.
[4] A.P. Godse, and D.A. Godse, Digital Principles & System Design, Technical Publications, pp. 180-188, 2009.
[5] R. Shalem, E.John, and L.John, "A novel low power energy recovery full adder cell," In Proceedings of Ninth Great Lakes Symposium on VLSI, pp. 380-383, 1999.
[6] N. Zhuang and H. M. Wu, "A new design of the CMOS full adder," IEEE Journal of Solid-State Circuits, vol. 27, pp. 840-844, May 1992.
[7] R. Uma, Vidya Vijayan, M. Mohanapriya, and Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies," International Journal of VLSI Design & Communication Systems, Vol. 3, No. 1, pp. 153-168, Feb 2012.
[8] A.M. Shams, T.K Darwish, and M.A Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, Issue 1, pp. 20-29, 2002.
[9] Kaushik Roy, and Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley Publications, 2000.
[12] Jasbir Kaur, and Lalit Sood, "Comparison Between Various Types of Adder Topologies," IJCST Vol. 6, Issue 1, Jan - March 2015.

[13] Saradindu Panda, A.Banerjee, B.Maji, and Dr. A.K. Mukhopadhyay, "Power and Delay Comparison in between Different types of Full Adder Circuits," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 1, Issue 3, September 2012.
[14] Sansar Chand Sankhyan, "Comparative Study of Different Types of Full Adder Circuits," Sansar Chand Sankhyan Int. Journal of Engineering Research and Applications, Vol. 3, Issue 5, pp.1062-1064, Sep-Oct 2013.
[15] Maroju SaiKumar, and Dr. P. Samundiswary, "Design and Performance Analysis of Various Adders using Verilog," IJCSMC, Vol. 2, Issue. 9, pp.128–138, September 2013.

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