

Review of Different Types of Power Efficient Flash Type ADC

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Abstract: This review paper inherits few different types of architecture for a low-power high speed Flash Analog-to-Digital Converter (ADC). Unlike conventional Full-Flash architecture in which power consumption is increased exponentially with the increase of resolution. New techniques adopted at the design level, such as the TIQ (Threshold Inverter Quantizer) structure and multiplexer in order to make the physical circuit very compact. In contrast with the traditional Flash ADC architecture that uses an area inefficient resistive ladder, 2^n-1 comparator, and an encoder, these design makes use of only a series of inverters and multiplexers. As a result, minimum power consumption would be achieved.

Keywords: Flash ADC, Low Power, Threshold Inverter Quantizer, sized threshold, Encoder.

1. Introduction

Analog signal are converted to the digital signal by the various architecture. Flash ADC is most suitable architecture which is used in analog to digital signal conversion because of its advantages. Flash ADCs are mainly used for high speed applications. Flash ADC consists of the various sections such as resistor ladder, Comparator array, Thermometer code to Binary code, encoder etc. The maximum power in the Flash ADC is consumed by the resistor ladder, and the encoder of the Flash ADC also consumes the significant amount of the power. So if the design of thermometer to binary code converter improves its power, the performance of the complete system is improved. With the advancement of technology, digital signal processing has progressed dramatically in recent years, it demands high speed and low power consumption ADC. By using the Threshold Inverter Quantization [1], we can eliminate the resistor array from the traditional Flash ADC through which chip-area and the power consumption is reduced.

There are different architectures proposed for the conversion of thermometer to binary code in the literature. Most common and widely used one is direct conversion of thermometer to binary code using 2:1 multiplexers. In this method the thermometer code is converted to binary using only 2:1 multiplexers [8]. This circuit is known for its high speed and low power consumption. The Flash type ADC is also known as the direct conversion ADC. The design process is also quite faster and cost effective.

2. Traditional Flash ADC

The traditional Flash ADC is designed by the series of the resistor ladder, comparator array, and the encoder as to convert the thermometer code to the binary code. There are 2^n resistors in the resistor ladder and 2^n-1 comparators are used in the comparator array. The input is given as V_{in} and the reference voltage is provided at V_{ref} . The V_{ref} comes to the input of the comparator generated by the resistor ladder. The number of resistors and the comparators used, can

increase exponentially with increase in resolution of the ADC

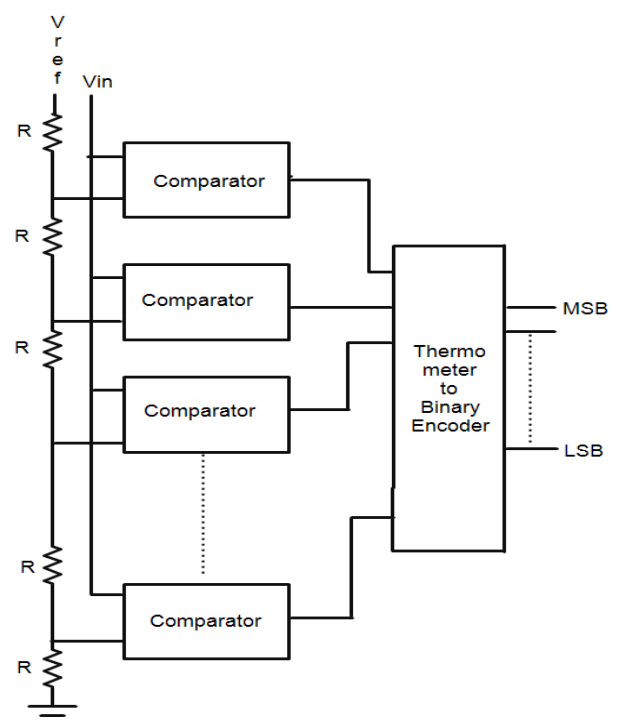


Figure 1: Traditional Flash type ADC Architecture

The output from the comparator array is known as the thermometer code. The thermometer code can be converted to binary code by using a Thermometer to Binary code encoder. The output of the encoder is the final output which is analogous to the analog signal given at the input. The Flash type ADC is also known as the direct conversion and it is a parallel ADC.

3. TIQ Based Flash ADC Architecture

Flash ADC architecture, also known as parallel ADCs, is the fastest among all other ADCs. In the Flash ADC, the input voltage compares with a set of increasing reference voltages by the Comparators. Comparators role is to convert an input

voltage (V_{in}) into a logic '1' or '0' by comparing a reference voltage (V_{ref}) with the V_{in} . If V_{in} is greater than V_{ref} , the output of the comparator is '1', otherwise '0'. The comparator output in digital signal known as Thermometer code, which can be easily converted into Gray code or the binary code depend on use. In the resistive flash ADC, the set of resistor is used to form the reference voltage and the comparator is used to compare the reference voltage with the input voltage and the output of the comparator is the known as the thermometer code. These thermometer codes are easily converted to binary code with the help of encoder. The difference in TIQ technique is the resistive network is replaced by the TIQ comparator. In TIQ technique each comparator is uniquely designed to set reference voltage internally. TIQ technique uses two cascaded CMOS inverters as a comparator [1]. The TIQ technique reduces the ADC chip area and power consumption as compared to the traditional flash ADCs. The Fig. 2 shows the block diagram of the TIQ flash ADC. The use of two cascaded inverters as a voltage comparator is the reason for the technique's name.

To provide full digital output voltage swing, we used gain boosters after comparator [2]. This is also use to make threshold of comparator output sharp.

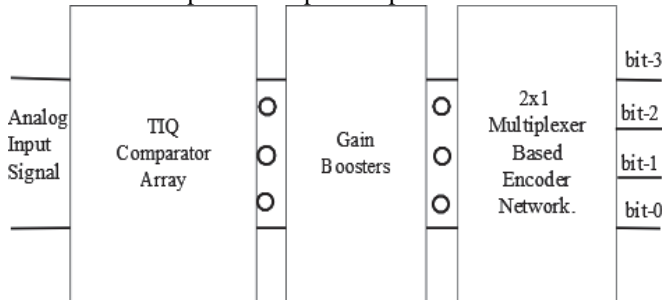


Figure 2: Block diagram of the TIQ ADC

D) TIQ Comparator

In TIQ technique each comparator is uniquely designed to set reference voltage internally. TIQ technique uses two cascaded CMOS inverters as a comparator [4]. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Hence, we do not need the resistor ladder circuit used in a conventional flash ADC. The gain boosters make sharper thresholds for comparator outputs and provide full a digital output voltage swing. The comparator outputs - the thermometer code are converted to a binary code.

The TIQ comparator consists two back to back CMOS inverter, connected in the series combination, for high speed and low power consumption. Threshold voltage of CMOS inverter is given by the equation:

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} (V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

Where,

u_n = Mobility of nMOS

u_p = Mobility of pMOS

V_{dd} = Supply voltage

V_{Tn} = Threshold voltage of nMOS

V_{Tp} = Threshold voltage of Pmos

So threshold voltages can be calculated by varying the Width W_p and W_n of pMOS and nMOS transistor respectively. So for a 4 bit ADC, 15 CMOS inverters are connected in parallel to examine input signal level.

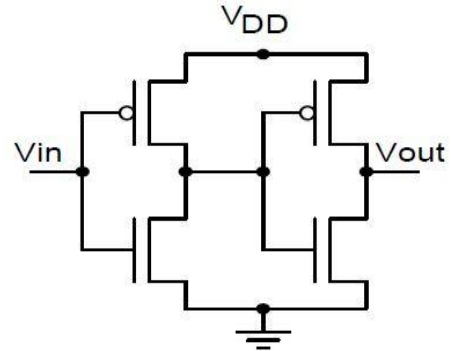


Figure 3: TIQ comparator.

II) Encoders of Flash ADC

The output of comparators is called Thermometer code. Sometimes the digital output from the comparator is ambiguous (neither 1 nor 0), the output is defined as meta-stable [3]. So somehow we have to reduce the meta-stability. The work done by Yang et al [3] shows that meta-stability can be reduced by using the Gray code because it allows more time for regeneration. We know that the Gray code encoding which allows only 1 bit in the output to change at a time is greatly improved meta-stability. Thus, the Thermometer code is first converted to Gray-code encoding and then later decoded to binary, if desired.

The literature of the encoder which is used in the flash ADC for low power dissipation and high speed are as follows:

A. Wallace tree based encoder

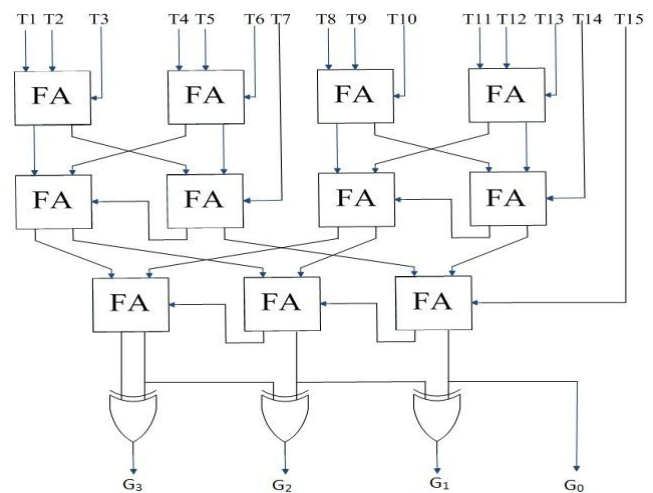


Figure 4: Wallace tree based encoder

Wallace tree based encoder is used to convert Thermometer code into Gray code. This encoding scheme is especially devoted to high speed analog to digital converters. It counts the number of 1's present in the Thermometer code [10]. Fig.4 shows Wallace tree based Thermometer to Gray encoder. The Wallace tree based encoder is built only with the elementary full adder cell. These 1 bit full adder cells is used to count the 1's occurred in the Thermometer code [6]. At the first stage each full adder cell counts the number of logical 1's at its entries and the output is 2-bit binary coded output. The second stage consists in adding the two-bit words of adjacent cells two by two, giving 3-bit binary outputs and so on in order to obtain the final binary output code for the converter. Finally the binary code is converted into the Grey code using XOR Gate. The number of full adder cells used in Wallace tree encoder is given by equation

$$m = 2^n - n - 1$$

Where m is the number of full adder cell for n-bit flash ADC. The main advantage of Wallace tree Encoder is that the encoded value can precisely match the best approximated output value. Wallace tree architecture is realized using Full Adder cells. This circuit contains more hardware and so the power consumption is high and speed is low. The disadvantage of this approach is that it results in large delay and power consumption [5] [6].

B. Fat tree based encoder

Fat tree architecture is more efficient way to convert the thermometer code to the Grey code. When we compare it with the Wallace tree based encoder it has its advantages as, in chip area and the delay. The Fat tree has smaller chip area and low delay. Fig. 5 shows the architecture of fat tree encoder for 15-bit thermometer code input [7].

A fat tree architecture is shown, which initially converts the thermometer code to 1 of N code to reduce the bubble error and then to Grey code using fat tree architecture. This circuit is also designed using basic logic gates. In this architecture the transistor count is high compared to other architectures.

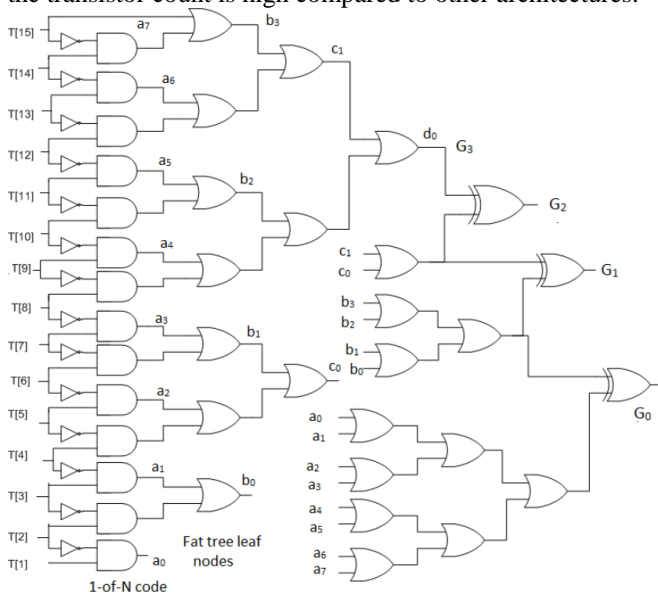


Figure 5: Fat tree based encoder

C. MUX based encoder

The most efficient approach to convert Thermometer code to the Grey code is a MUX based encoder [8]. As we compare to Wallace tree based encoder and the Fat tree based encoder, it results in the high speed and the smaller chip area. Fig. 6 shows the architecture of MUX based encoder for 15-bit thermometer code input.

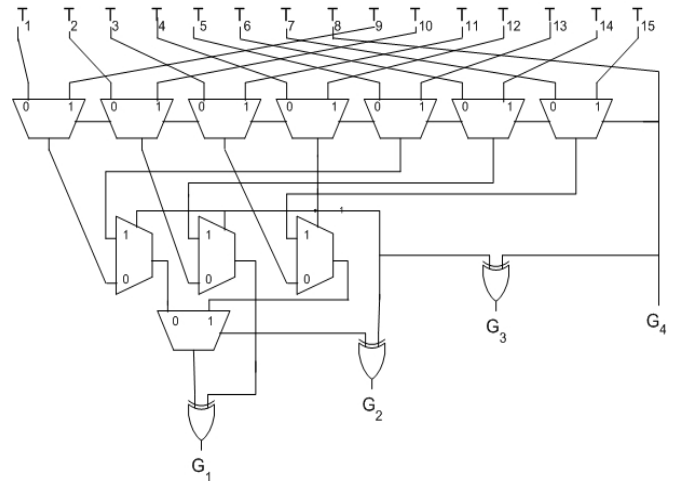


Figure 6: MUX based encoder

4. Comparisons of Encoder

Table 1: Comparison of encoder For 31-Bit

	Delay (ns)	Area. (um ²)	Power (mW)	Figure of Merit (fJ)
Wallace Tree	8.977	13520	0.623	5592.671
Fat tree	8.498	6984	0.217	1844.07
MUX tree	7.540	3696	0.216	1628.64

Wallace tree architecture is realized using Full Adder cells so this circuit contains more hardware and so the power consumption is high, area is large and delay is more compare to other architecture for the encoder as shown in the table [9]. On the other hand the delays of the MUX tree his lowest among the all because of the tree structure, area of the Wallace tree and the Fat tree is larger as compared to MUX tree. Similarly other parameter of the encoder like power consumption and figure of merit in the MUX tree are low as compared to the other tree architecture. The Graphical depiction of power consumption and the delay of these trees is shown as,

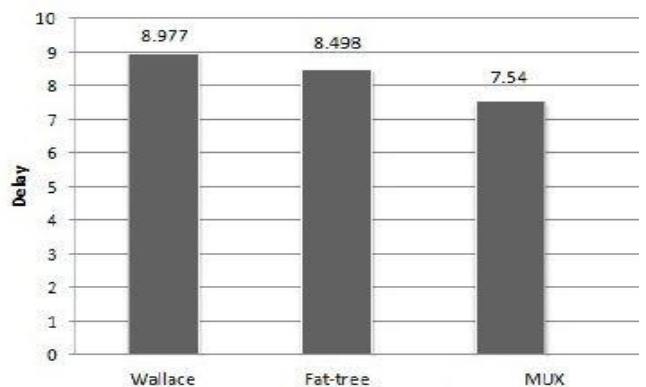


Figure 7: Delay comparison of encoders

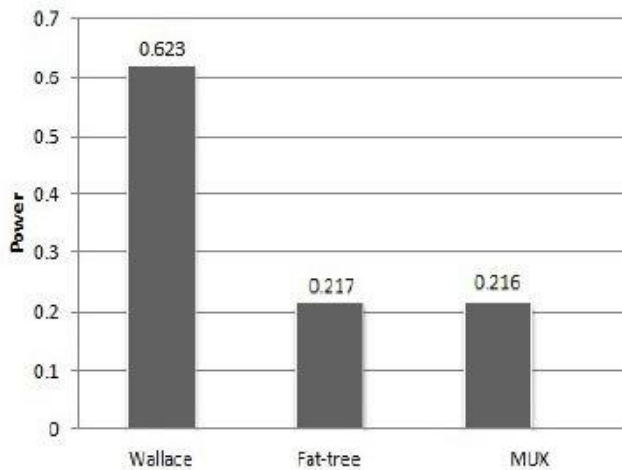


Figure 8: Power consumption of different encoders

5. Future Work

Above described circuits were few flash ADC circuits. These all have some advantages and disadvantages. Future work must contain regarding the improvement of previous given circuits. The parameters like power dissipation of overall circuit, output power, threshold current, efficiency of the circuit, delay etc should be of main concern when they will be studied.

6. Conclusion

The TIQ based Flash type ADC described in this paper is a summarized form of different Flash ADC circuits. This paper shows a hierarchy of Flash type ADC circuits from earlier to current work in this area.

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