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Design and Implementation of QSD Adder using Quaternary Logic Lookup Table Based on Standard CMOS Technology

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Abstract: ***Multiple-valued logic (MVL) based quaternary look-up-table (QLUT) approach along with QSD adder is proposed in this paper to achieve high performance. The designs in the proposed method are designed to overcome the issues in the existing methods such as extreme power consumption, chip size, delay and increased interconnections in accurate manner. Increasing interconnections and switch resistant based problems in standard CMOS structure are effectively handled by QLUT based clock boosting technique which operates based on MVL. QSD adder is the additional contribution to MVL based QLUT to improve the performance with great reliability. MVL based QLUT-QSD adder approach is valid solution to existing problems. A carry-free arithmetic operation can be achieved using a higher radix number system such as Quaternary Signed Digit (QSD) "The Proposed method can improve the time consumption, power consumption and accuracy by exploiting the redundancy. Experimental results reveal that proposed QLUT-QSD adder achieves low computational cost, low power consumption and better accuracy over traditional BLUT***.

Keywords: Multiple valued combinational, quaternary look-up-table, QSD carry free adder, Clock boosting technique, Binary look up table

1. Introduction

Technology transformation have observed immense growth in the field of digital circuitry while transforming from continuous based analog systems to non-continuous based digital systems. A modern integrated circuitry came into existence which has created a revolution in digital circuitry and implementation of integrated circuitry is popularly known as Very-large-scale integration (VLSI). The integrated circuit size is consistently declining over the years and with the introduction of VLSI it reaches to next level. Designing a VLSI circuit system based on silicon CMOS technology has ability to attain high performance and low computational cost.

CMOS digital circuit design is composed of various parameters and major part of integrated circuit is dominated by interconnections with almost 90% margin compared to rest of the parameters. Interconnections are vividly used in integrated circuit (IC) to transfer the information between transistors but its impact on remaining parameters force the researchers to develop new technology which should have ability to cope with the interconnections issues. Multi valued logic (MVL) is designed to decrease the power consumption which eventually decreases the interconnections and it is strongly supported by various VLSI standards around the globe. The Standard CMOS technology usage in digital circuitry has increased and the entire processing architecture of proposed method is designed based on it, its primary characteristics are time and power respectively.

Multi valued logic (MVL) approach is designed to cope up with all interconnections related issues in accurate way. MVL is presented in novel way along with quaternary look up table design to design voltage-mode standard CMOS circuits and improvised switching operations are carried out based on simplified clock boosting (CB) technique. The traditional binary logic is replaced by proposed quaternary logic based MVL LUT system but design model is simple so in proposed methodology both logics belongs to quaternary and binary are combined efficiently and both use the same fabrication technology. A standard 130-nm CMOS technology with 1.2 V is implemented in this work which is further used for circuit fabrication.

2. Related Work

A. History of VLSI

VLSI circuit designing is considered as alternative to traditional circuit design systems in terms of size and as well as cost. It has created technological revolution in the design of integrated chip design and reaches to new level with its ability to combine billions of transistors with less size and low computational cost. The history of VLSI starts at late 1940's with the invention of transistor by BELL laboratories and the development done in this field is entirely gives credit to inventor of transistor. The different phases of VLSI in different times are as follows

- Invention of transistor is inspired JACK KILBY to invent first integrated circuit (IC) in late 1950,s at TI
- Small Scale Integration (SSI) implementation in early 1960's starts the combination of different transistors to form an integrated circuit and in history it is considered as first work in integrated circuit development with 10's of transistors on chip
- Small Scale Integration (SSI) followed by medium scale integration process in late1960's with ability to combines 100's on chip

- VLSI implementation in early 1970's for digital circuit design is an landmark inventive implementation which has ability to integrate 1000's of transistors on chip and reaches 1,000,000s till early 1980's. The increasing number of transistors eventually decreases the IC size and IC cost with large margin.

B. Quaternary Logic

The logical operation of quaternary logic design is based on multiple-valued logic and it is considered as constituent of multiple-valued logic which flourished with various advantages. Implementation of multi-valued systems results in less number of interconnection lines and processing elements. The representation of logic circuits of quaternary is less compared with traditional binary system, example: The representation of decimal number '255' is observed two different versions for binary and quaternary, in quaternary logic it is represented as '3333' while in its counterpart binary logic it is represented as'11111111'. Choosing radix value is one aspect where quaternary logic attains good results over traditional binary logic and the choice of radix is classified in actual and conceptual domain. Quaternary logic takes various parameters into account such as voltage, current, charge etc before choosing one domain from actual and conceptual domains.

Quaternary logic is simple in nature and it maintains its simplicity even in implementation of it on available circuitry and the implementation process is accomplished without taking additional components into consideration. The logic circuits belong to quaternary logic in designed to realize the quaternary

C. Look up tables

Memories are essential element of digital circuitry and look up tables (LUTS) is regarded as fast memories whose implementation is accomplished as logic function is done based on their selection mode. LUT comprise of memory cells which is used to implement small logic functions in reliable manner. SRAMS and FPGA's make use of LUT logic in them to accomplish the tasks based on them. Each LUT element has combination of single bit memory cells on which individual bit values are saved as storage system in every LUT element. The configuration values has very important role and they are initially stored in the look-up-table structure and once the input values are assigned to it the SRAM logic value is occurred as resultant outcome as output.

The representation of look up table capacity $|C|$ is given by

$$|C| = n \quad b^k \qquad (3.1)$$

The input is represented by 'k'; its respective outputs are represented by 'n' and 'b' variable represents the logic values. The binary look-up-table with 4 inputs and one output has ability to store 16 Boolean values i.e. $^4 = 16\ boolean\ values$. Binary look-up-table functions are represented as $|F|$ with 'k' input variables is given by

$$|F| = b^{|C|} \qquad (3.2).$$

The comparative analysis between binary look up table (BLUT) and quaternary look up table (QLUT) in terms of capacity is shown in following tabular column.

Table 2.1: Comparative analysis between binary look up table (BLUT) and quaternary look up table (QLUT)

Parameter	BLUT (2 variable, 1 output)	QLUT (2 variable, 1 output)
Capacity: $\|C\| = n \quad b^k$	$\|C\| = 1 \quad$ =4 2 i/p BLUT: holds 4 logic value	$\|C\| = 1 \quad$ 4=16 2 i/p BLUT: holds 16 logic value
$\|F\| = b^{\|C\|}$	$\|F\| = \ ^{\|4\|}$=16	$\|F\| = 4^{\|16\|}$=4294967296

Table 2.2: The comparative implementation of BLUT and QLUT in terms of any 4 variable functions

Parameter	4 i/p BLUT)	2 i/p QLUT
Capacity	Stores 16 logic values	Stores 16 logic values
Inputs (Select lines)	4	2
Transistor count with transmission gates	34 NMOS, 34 PMOS	42 NMOS, 42 PMOS
Total number of nodes formed	15	5
Multiplexer stages	4	2

D. Interconnections

The structural representation of FPGA structure is a combinational structural unit composed of fully programmable network which consists of Input/Outputs (IOs), Configurable Logic Blocks (CLB) and remaining components of FPGA too taken into consideration. Different interconnections are tested and implemented foe providing efficient FPGA routing algorithms implementation. Example based explanation of interconnections are explained as follows

Example

Xilinx Spartan-3 FPGAs is interconnected with four types of interconnections namely long lines, hex lines, double lines and direct lines. Various FPGA based techniques are implemented in literature based on interconnections and by using these techniques a model is designed as distributed RC networks using the Predictive Technology Model (PTM) parameters for a 45nm technology.

Interconnections impact on FPGA performance

Although quaternary LUT has various advantages over binary LUT but still increased propagation is considered as major drawback in Quaternary LUT when compared with its counterpart. Reduction in look-up-tables is done by quaternary LUT which provides smaller wires and which is further used for circuit functions implementation

3. Importance of Multiple-Valued Logic (Mvl)

The field of digital-computing machinery has been dominated by two valued signals for most of the time and it has ability to support only two radices which proved to be inefficient for modem day applications. Binary representation of data needs. Although tremendous progress has been made in the past but no such logic is designed to replace the binary logic till MVL came into implementation. The dominance of binary logic is continued with MVL in modified manner, where binary logic has two states while its alternative MVL is composed with finitely or infinitely numbers of values. The journey of MVL is not new and its representation with different technologies are illustrated in fig.3.1 as follows

The implementation of MVL system is initially started with FPGA which is followed by MVL-Multiplier, MVL- Adder and finally MVL-Look up tables; MVL is adaptively changes itself according the technology to support large range of applications in modern world.

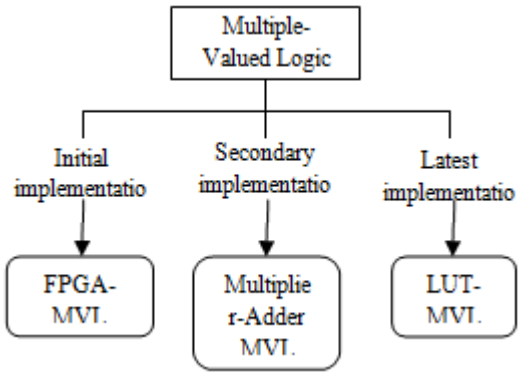

Figure 3.1: Multiple-Valued Logic (MVL) Implementations

A. Reduced number of operations by MVL

Operational mechanism of multiple-valued logic has in-built design which is designed to operate with a radix value more than two. Digital processing algorithms and frameworks consumes large amount of power and implementation of MVL in it has increased the opportunities to design new applications than its predecessor binary logic. Increased number of operations halt the performance in traditional binary logic based digital processing algorithms (which has two operations ‖true‖ and ‖false‖)while it is effectively handled by MVL to get optimal performance as outcome with reduced number of operations. The computational process based problems in digital systems needs special attention from researchers to find better alternatives in order to solve the problems with ease. MVL implementation in digital simplifies the computational processing of the system by reducing the number of operations and creates the ample platform to understand the problem in depth before predicting the solution which increases accuracy and reliability.MVL proposed solutions are more efficient than traditional binary system and depth analysis is considered as major difference between the both systems. The comparison of MVL with binary logic is represented in following tabular column

Tabular column 3.1: Binary logic vs Multiple-valued logic

Contents	Binary Logic	Multiple-Valued Logic
Interconnections	More compared with MVL	Less compared with binary logic
Logical states	Only two	More than two
Time, power and area	More compared with MVL	Less compared with binary logic

B. Applicative advantages of MVL over binary system

Design of digital has great prominence in modern world which led way for designing more and more technologies to cope with problems in efficient manner but traditional binary systems fails miserably while proposed MVL systems is highly successful with inscription of multilevel signals in design of digital systems. The additional opportunities offered by MVL system is as follows

- Pin-Out problem: It is considered as common problem arises in traditional binary system because of large number of interconnections in system design and external connections with devices. MVL solves the pin-out problem with ease by reducing the interconnections as well as connections with external devices.
- Ripple-through carriers: Arithmetic operation (binary addition and binary subtraction) are performed with decreased ripple-through carriers in equipped manner. Increasing ripple-through carriers has adverse impact on performance of the system which is designed to meet the realistic applications.
- Inclining behaviour of packing density: We stress the point that the Quaternary signals conversion is applied only when the arithmetic operations needs to perform in equipped manner. Otherwise the Quaternary signals conversion is not required.

4. Proposed Method

The proposed quaternary variable is comprises of two techniques (i) Clock boosting approach for optimize switch resistance and (ii) QSD adder for achieving high performance. Binary variable used to carry less information in its system which is a concerned area in circuit design and implementation of quaternary logic in digital systems is designed with a system with ability to carry the two times more information than the traditional binary variable. Quaternary logic (Q) variable is design to assume four different logics with three different voltage ranges and four noise margins to determine the quaternary value. The representation of quaternary variable (Q) is as follows

$$|Q| \qquad |B| \quad (4.1)$$

The quaternary variable is composed of two binary variables and two binary nodes are grouped to form a quaternary node as shown in formula 4.1. Grouping the two binary variables is to avoid the information loss in implementation.

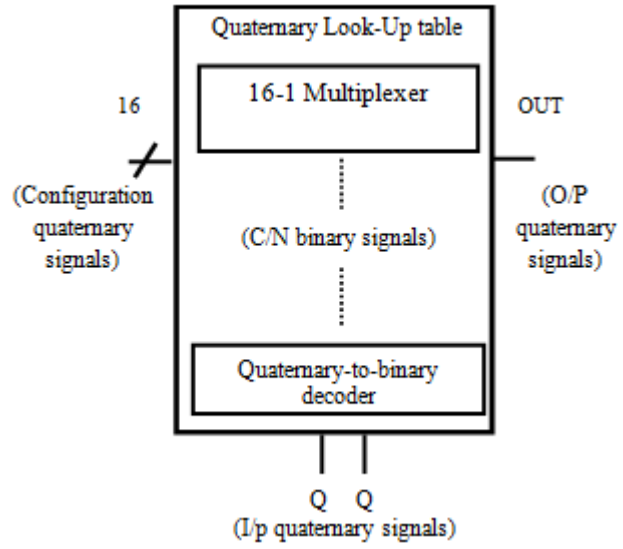

Figure 4.1: Quaternary binary look-up table (QLUT)

The implementation of standard CMOS approach in proposed work is useful to convert the BIN to QUAT conversion while traditional CMOS systems lacks of this. Intense research is carried out in the literature on the BIN to QUAT conversion along with quaternary implementation for LUT too carried on side by side. Look up table based quaternary logic has increased the ability of system to carry the information. Look up table implementation with

quaternary logic with the specified number of inputs and outputs have the ability to support various practical applications in terms of designing and implementation on hardware.

(a) QLUT Methodology and Implementation

Quaternary look up table (QLUT)is proposed with 2-input and 1-output in this work and its pictorial view is presented in Fig.4.2. An intelligent work is carried out in this work,16 different configurations are taken as inputs, two quaternary inputs are combined to form one possible combination. The configuration inputs are necessary to accomplish the QLUT logic in practical approach. The proposed work comprises of two blocks, (i) a low resistance path is designed in between the switches to carry the data in hassle free manner and 16 multiplexers based low resistance path is designed based on array of switches. (ii) Another block is 2-bit ADC (analog-to-digital) combinational based quaternary decoder.

(b) 16-1 multiplexer

The quaternary nature of 16-1 multiplexer inputs in Fig.4.2 makes it appear like analog multiplexer. 16-1 multiplexer output value is assumed as capacitive one and its value is analyzed by interconnection network to which QLUT output is connected. QLUT reduces the number of wires used for interconnections which decrease the size makes it look like compact which in-turn reduces the routing capacitance and another additional feature inscribed a binary typical value to add additional functionalities without increasing the number of wires.

Traditional QLUT approach based multiplexer path is implemented by transmission gates which consumes more power and time. Switch resistance is reduction is helps to reduce the propagation delay. Traditional QLUT systems uses two switches inside multiplexer while in proposed method one switch is used in place of two switches.

(C) Clock boosting technique

The QLUT design based on transmission gates suffer from high power consumption and abnormal switch resistance. The proposed QLUT design has ability to handle the switch resistance in reluctant manner and power consumption is efficient way. The proposed method utilizes the clock boosting technique in place of traditional transmission gates approach to reduce the power consumption by decreasing the number of interconnections.

(d) Q2B decoder

Control signals 16 are generated and applied to CLK 1 inputs of each switch because the 2-bit quaternary-to-binary decoder will allow the use of single row of switches to drive the input configuration signals to the output of the QLUT. These switches are used to connect one quaternary configuration input to the output. For the generation of required control signals, binary logic gates are employed to decode quaternary variables into binary. Thus, an ADC frontend is necessary, considering the analog nature of the quaternary signals.

(E) QSD ADDER

Binary arithmetic operations are mainly performed with carry propagation delay of$o(n)$, which is very high and considered for research issue. But with the help of carry lookahead propagation delay is reduced to the lowest value of$o(logn)$, but it is bounded to very less number of digits due to the complexity. Both the above systems having some drawbacks to overcome the drawback of carry we are going for carry free arithmetic operations adopting higher radix number system such as Quaternary Signed Digits (QSD). In QSD we are representing any digit between -3 and 3. Adapting this type of system we are getting results without ripple carry which also provide a fixed delay and independent of the number of digits. So that we are easily getting a system operating on huge number of the digits and provides constant delay and less computational complexity.

5. Results and Analysis

A. Existing System

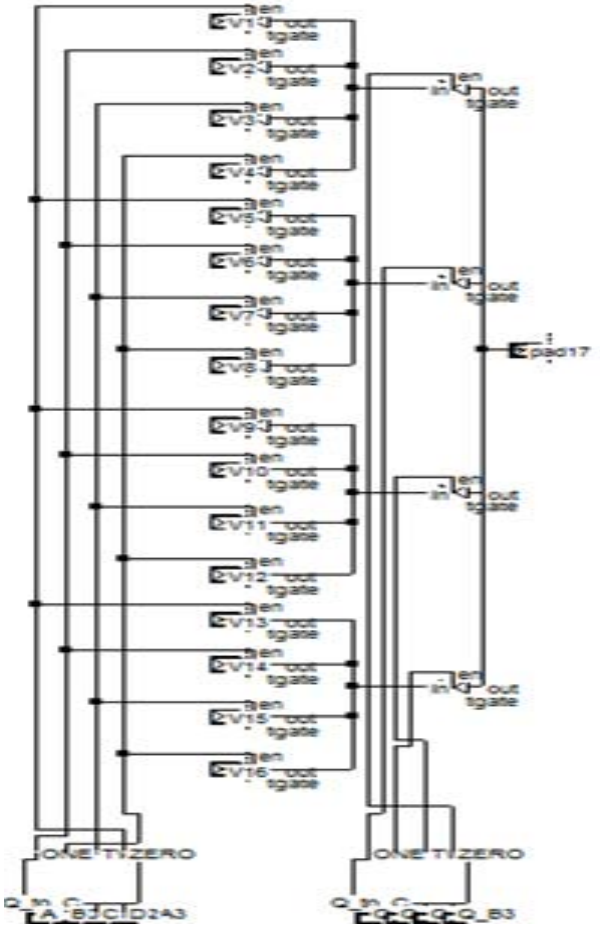

Figure 5.1: QLUT schematic representation based on traditional transmission gates

Analysis

Transmission gates used in traditional QLUT design is shown in above figure where 16 transmission gates are used. Every four gates are combined to form one block and four blocks are formed which are used to control the capacitance but heavy consumption remain as issue in this.

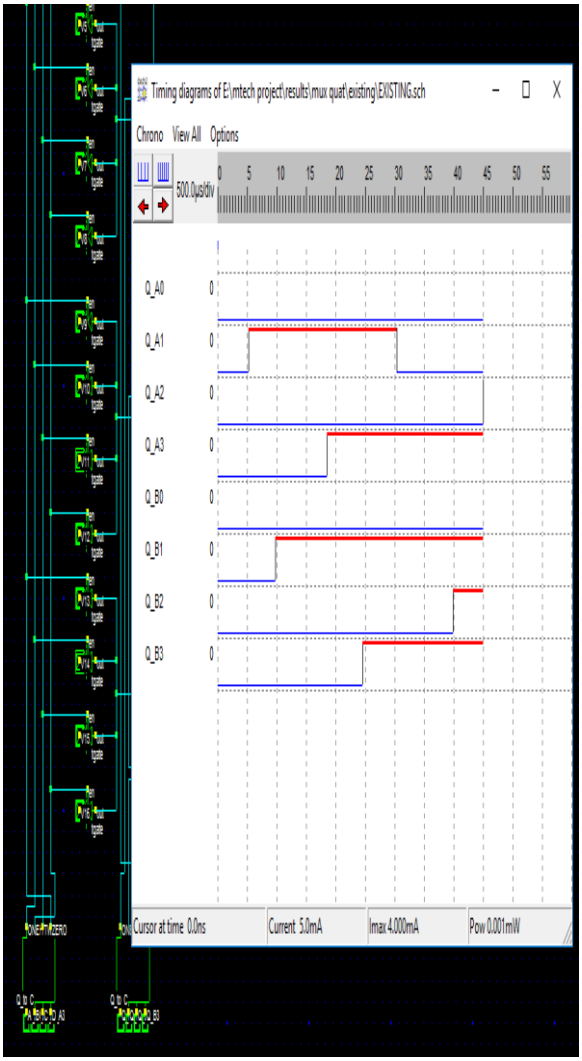

Figure 5.2: Figure of QLUT Transmission gates result

Analysis

Traditional QLUT logic result is depicted in above figure. The result of transmission gates is included with 16 transmission gates. Different timing values are used in the results to handle the propagation delay along with the power consumption but large number interconnections remains as unresolved issue in it. Power consumption of existing system shown in above figure

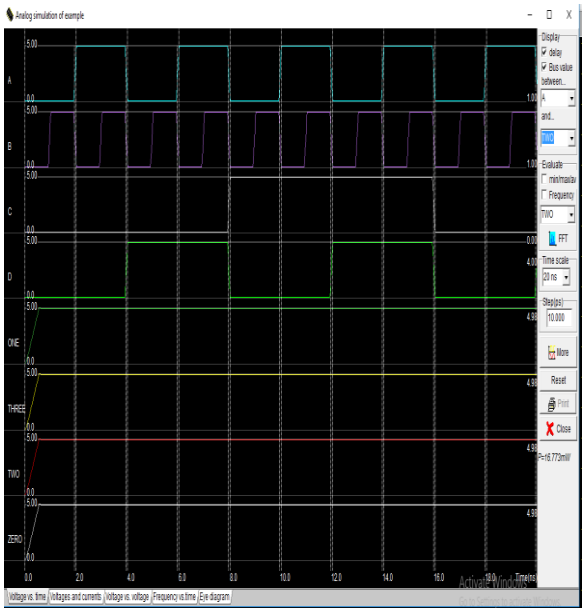

Figure 5.3: Figure of QLUT Transmission gates power consumption

Analysis

Power consumption remained as un-resolved issue in traditional binary system which is effectively handled by transmission gates based QLUT design and it is improved in accurate manner in proposed QLUT-QSD design

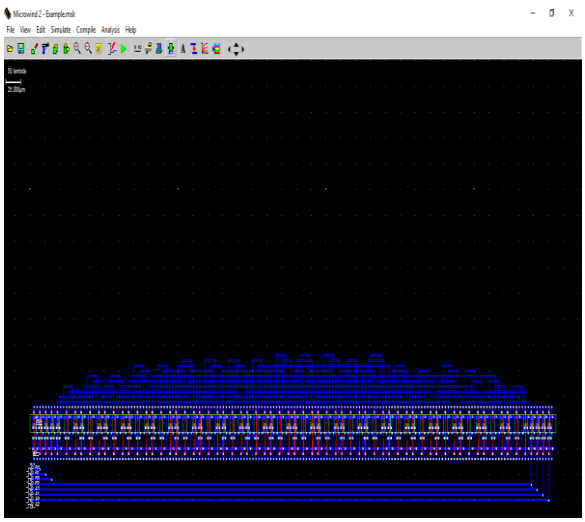

Figure 5.4: Figure of existing transmission gates QLUT Transmission layout

Analysis

Transmission gate usually acquired better results than binary system but still needs improvement. Layout representation of traditional QLUT system is shown in Fig. 5.4

B. Proposed System

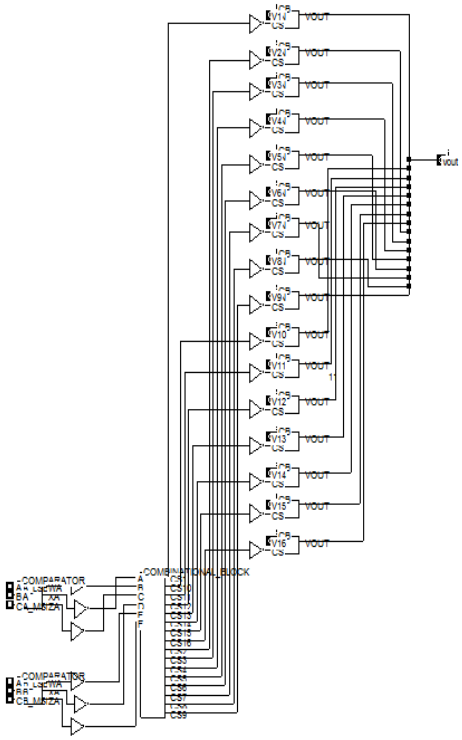

Figure 5.5: Figure of QLUT Transmission gates power consumption

Analysis

The proposed QLUT logic schematic figure is shown in above figure with different design than existing. The clock boosting technique with novel QLUT design helps to reduce the interconnections and delay with reliable accuracy.

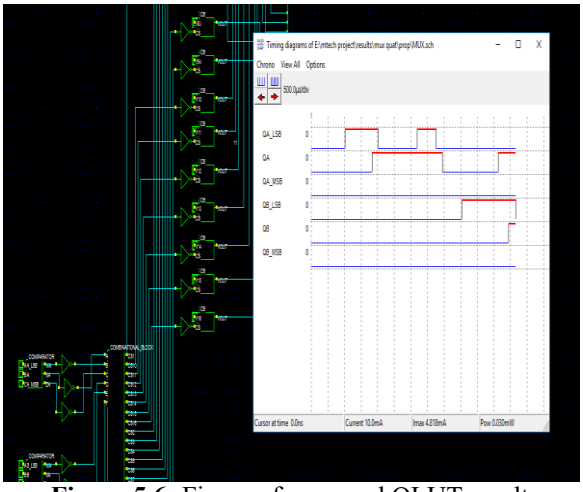

Figure 5.6: Figure of proposed QLUT result

Analysis

The proposed MVL based QLUT algorithm is logic implemented in this work and the associated result is depicted in above figure. The proposed method result is comprises of different techniques and its result is shown in above figure

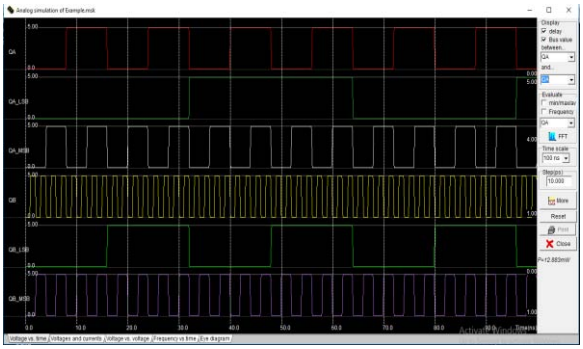

Figure 5.7: Power consumption of MVL QLUT

Analysis

Power consumption problem is efficiently solved in proposed system by reducing the interconnections in MVL QLUT logic which increases accuracy than its counterpart i.e. existing systems.

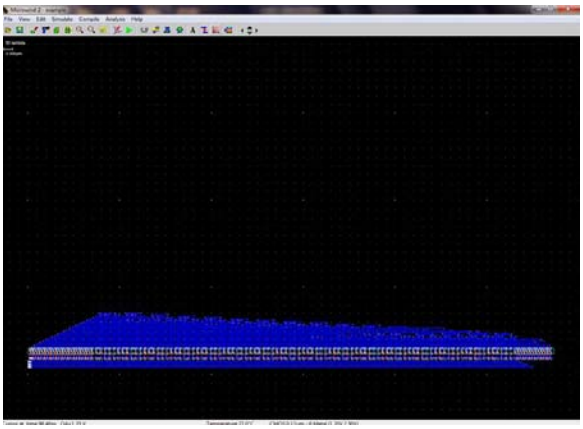

Figure 5.8: Figure of proposed standard CMOS based QLUT layout

Analysis

Clock boosting technique usage acquired good results than existing with good improvement in terms of interconnections. Layout representation of traditional QLUT system is shown in Fig. 5.8

C. Contribution

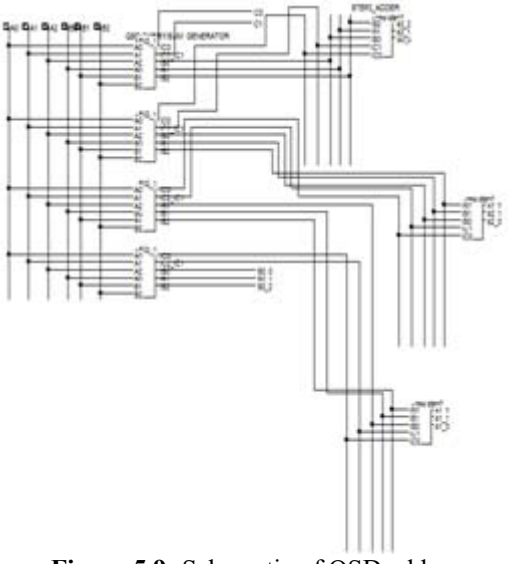

Figure 5.9: Schematic of QSD adder

Analysis
The QSD adder is continuation to proposed QLUT logic schematic figure is shown in above figure with different design than existing. The clock boosting technique along with QSD adder helps to reduce the interconnections and delay with reliable accuracy.

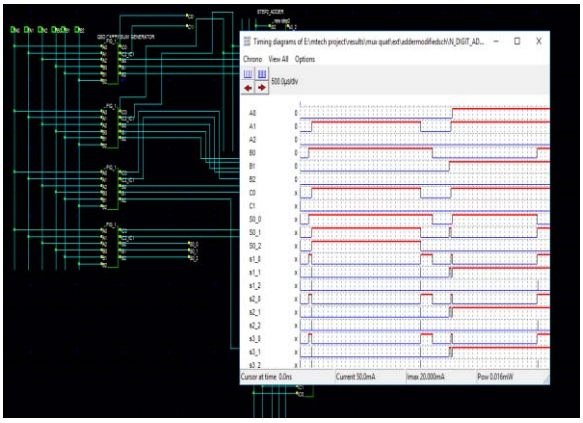

Figure 5.10: Result of QSD adder

Analysis
The proposed MVL based QLUT algorithm along with QSD adder is implemented in this work and the associated result is depicted in above figure. The proposed method result is comprises of different techniques and its result is shown in above figure

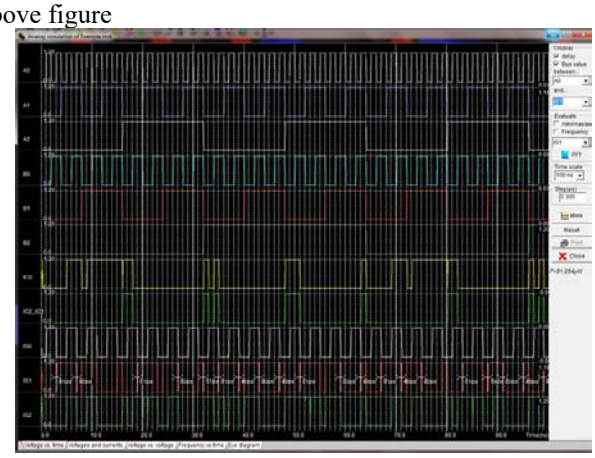

Figure 5.11: Power consumption of QSD adder

Analysis
Power consumption problem is efficiently solved in proposed system along with QSD adder by reducing the interconnections in data transfer which increases accuracy than its counterpart i.e. existing systems.

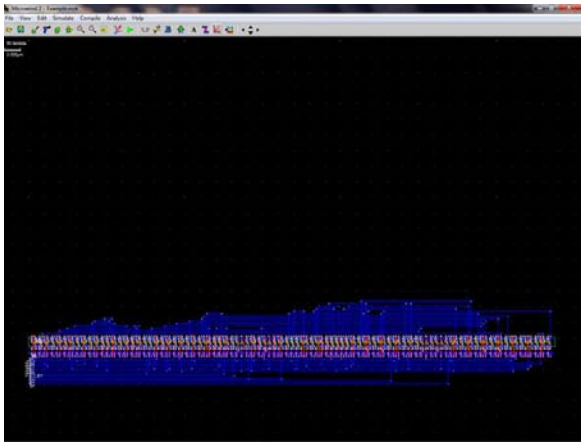

Figure 5.12: Figure of proposed standard QSD adder

Analysis
Clock boosting technique along with QSD adder usage acquired good results than existing with good improvement in terms of interconnections. Layout representation of traditional QLUT system

6. Conclusion

Technology constantly changes its facet along with time. Consistent improvement has led for the creation of advance algorithms to solve the existing issues with ease. VLSI industry has registered tremendous growth last few decades in with decline in circuit size and increased interconnections. Interconnections are increased pose serious issues and addressed the issues of interconnections in this work with development of novel approach. The interconnections have its impact on performance. The proposed method design is comprises of switch resistant algorithm (clock boosting) and an additional adder (QSD adder) to enhance the performance and accuracy in reliable manner. The experimental results had shown its supremacy over conventional state-of-art methods.

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Dr. M. Gurunadha Babu is a scholar with rich industry experience. He has 22 years of industrial and academic experience. He has worked as Associate Professor and Head of ECE department in various Engineering colleges under JNTUH such as Chilkur Balaji Institute of Technology and JBIET. His industry experience includes working as senior Engineer, in Telecom Domain, in Avantel Communications Limited, involved in the production of MARR Telecom Systems. He has coordinated many workshops and contributed 11 papers to various International Journals. He also has to his credit the award of Best Lecturer 3 times.