Design and Implementation of Power Efficient 8:1 Multiplexer Based on Adiabatic Logic

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Abstract: *The increasing speed and complexity of today's designs implies a significant increase in the power consumption of the very-large scale integration (VLSI) of chips. To meet this challenge, researchers have developed many different design techniques to reduce the power. Adiabatic switching principle is one of the important circuit design technique, which reduces the power consumption compared to conventional CMOS. This paper presents a 8:1 multiplexer based on adiabatic switching principle that uses a pair of complementary split-level sinusoidal power supply clocks for digital low power applications. Some standard adiabatic logic styles like PFAL, ECRL, 2n2n2p are investigated, but the proposed logic is better. The simulation is carried out in TSPICE software at 0.5 μm CMOS technology for frequency range 200MHz – 800MHz.*

Keywords: Adiabatic logic, Multiplexer, PFAL, ECRL, 2n2n2p, power dissipation, power saving

1. Introduction

With the widespread use of mobile, hand-held and wireless electronics devices, the demands for the innovations of low-power VLSI arise. For most of the digital circuits today, CMOS logic scheme has been the technology of choice for Implementing low-power systems. As the clock and logic speeds increase to meet the new performance requirements, the energy requirement of CMOS circuits are becoming a major concern in the design of these devices. The word adiabatic comes from a Greek word that is used to describe the thermodynamic processes. In thermodynamic process, there is no heat exchange with the environment and therefore, no energy loss in the form of dissipated heat.

In real life computing, such ideal process cannot be achieved because of the presence of the dissipative elements like resistances in the circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as recovery CMOS [1].

Adiabatic logic has an important advantage over the conventional CMOS, i.e. the power dissipation in the adiabatic logic is less compared to conventional CMOS.

Each power-clock cycle, as shown in fig.1, consists of four intervals. In the evaluate (E) interval, the outputs are evaluated from the stable input signals. During the hold (H) interval, outputs are kept stable for supplying the subsequent gate with a stable input signal. Energy is recovered in the interval called recover (R). And for symmetry reasons, a wait (W) interval is inserted, as symmetric signals are easier and more efficient to be generated.
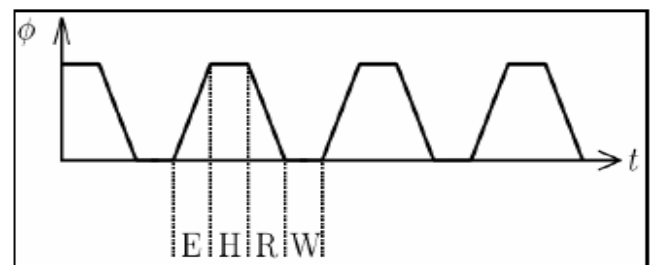

Figure 1: Scheme of the four phase power clock

In this paper, the standard adiabatic logic styles, which have been investigated are: ECRL [2] [3] [6], PFAL [2] [4] [6] and 2n2n2p [2] [5] [6]. Their general schematics are given in fig. 2, 3 and 4.
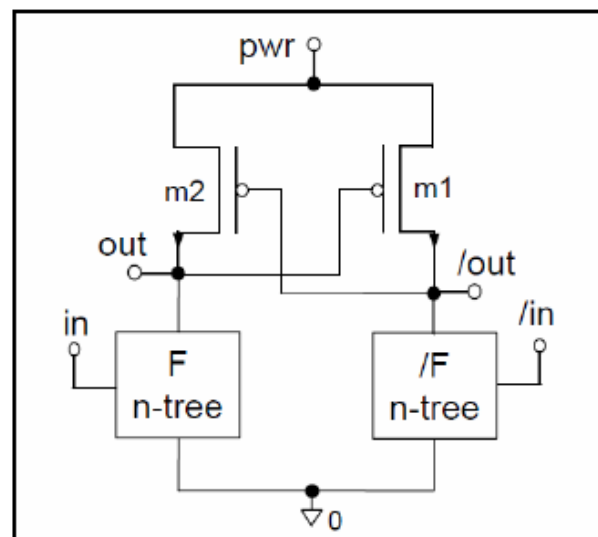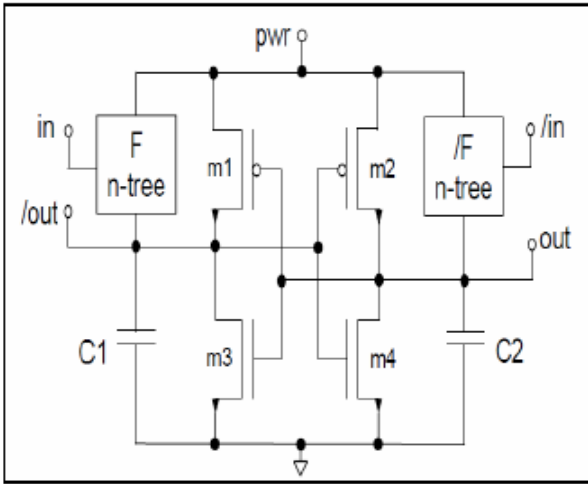

Figure 2: Schematic of ECRL

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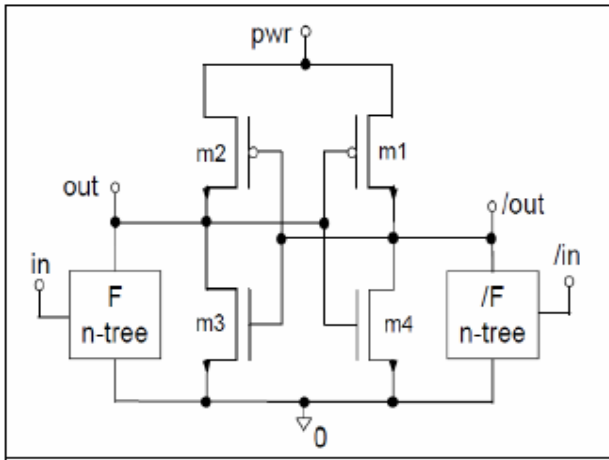
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Figure 3: Schematic of PFAL

Figure 4: Schematic of 2N2N2P

This paper analyses the total power dissipation of the multiplexer circuits using the standard logic styles and proposes a new logic style with lesser power dissipation.

2. Expressions of Multiplexer

A multiplexer is a special type of combinational circuit which selects only one of „n‟ given data inputs and routes it to the output. The selection of one of the inputs is done by „m‟ select inputs, with $2^m = n$.
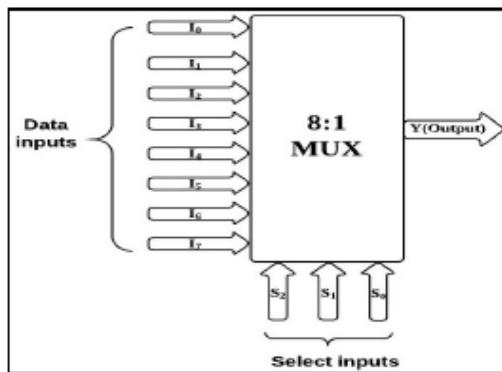The block diagram of 8:1 multiplexer is shown in fig. 5.

Figure 5: Block diagram of 8:1 multiplexer

Its truth table is given in table 1.

Table 1 8:1 Multipleexer Truth Table

Select Inputs			Outputs
S2	S1	S0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

From the truth table output expression can be given as:

$$Y = \overline{S}_2 \overline{S}_1 \overline{S}_0 I_0 + \overline{S}_2 \overline{S}_1 S_0 I_1 + \overline{S}_2 S_1 \overline{S}_0 I_2 + \overline{S}_2 S_1 S_0 I_3$$
$$+ S_2 \overline{S}_1 \overline{S}_0 I_4 + S_2 \overline{S}_1 S_0 I_5 + S_2 S_1 \overline{S}_0 I_6 + S_2 S_1 S_0 I_7.$$

3. Logic for Proposed Circuit

The first difference between proposed circuit and static CMOS logic gate is the two diodes, one from the output node to the power clock supply and another one is placed next to the NMOS logic to another power clock. Both MOSFET-diodes are used to re-cycle the charges from the output node, to improve discharging speed of internal signal nodes.
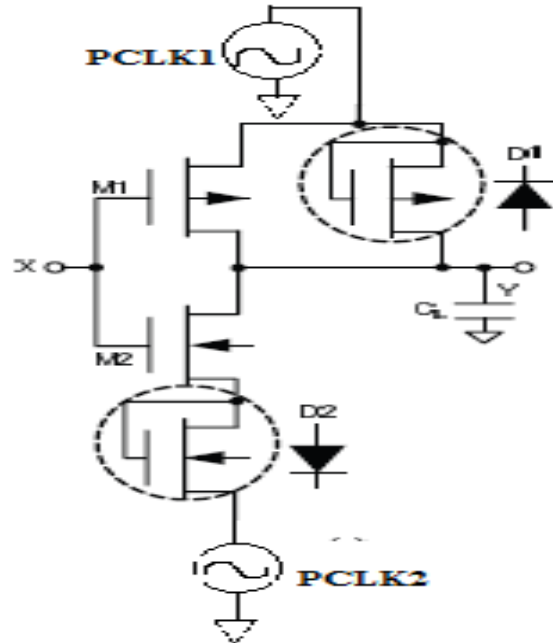

Figure 6: Proposed inverter circuit

In this inverter circuit, two sinusoidal power clocks are used, which are out of phase. During the evaluation phase of the power clocks, the potential difference is maximum between the power clocks and load capacitor is charged up to peak value and output is obtained. In the hold phase of the power clock, the charge from the load capacitor is recovered. In this way energy is recovered from the output node.

4. Proposed 8:1 power efficient adiabatic multiplexer

Figure 7 shows the proposed power efficient multiplexer based on the adiabatic logic. The simulation of the proposed logic for the multiplexer against the standard logic styles- PFAL, ECRL and 2n2n2p have been done with load capacitance 10fF at a frequency range 200-800 MHz. Their power consumptions are carried out at 0.5 μm technology with W = 1.25μm and L = 0.5μm, VPCLK = 3.3V, V= 3V (the input pulse voltage).
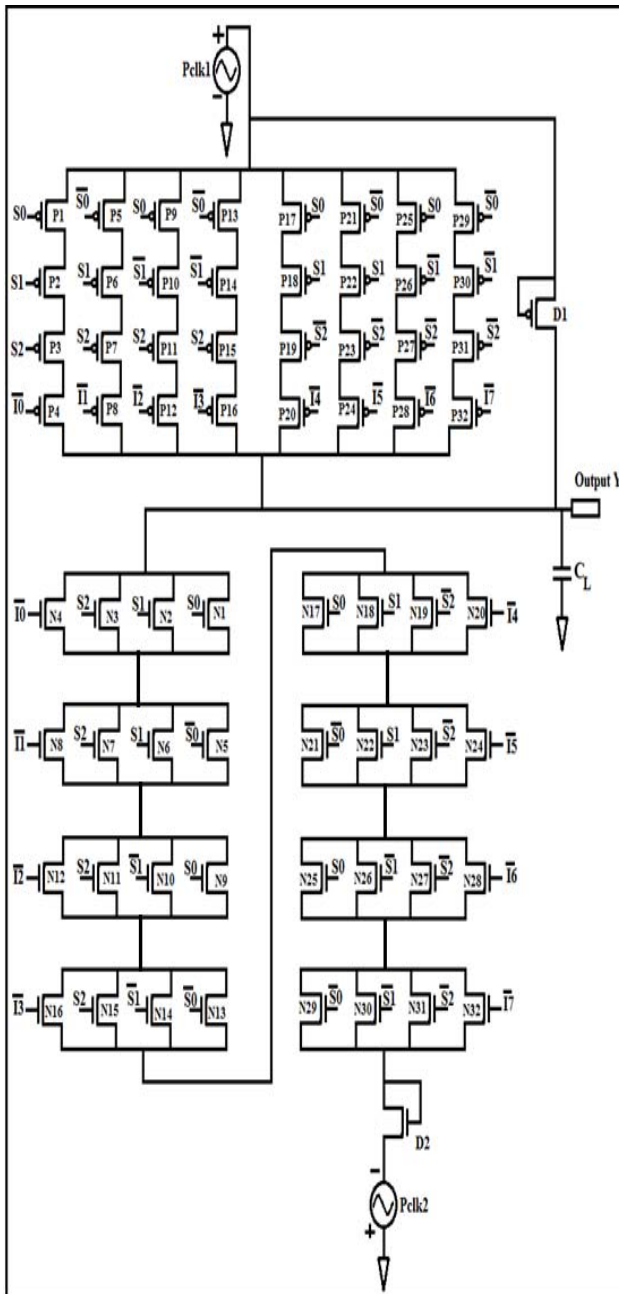

Figure7- Proposed circuit for 8:1 multiplexer

5. Simulation Result for Proposed Multiplexer

Figure 8 shows the simulation results of the proposed 8:1 multiplexer based on the adiabatic logic. After simulation,

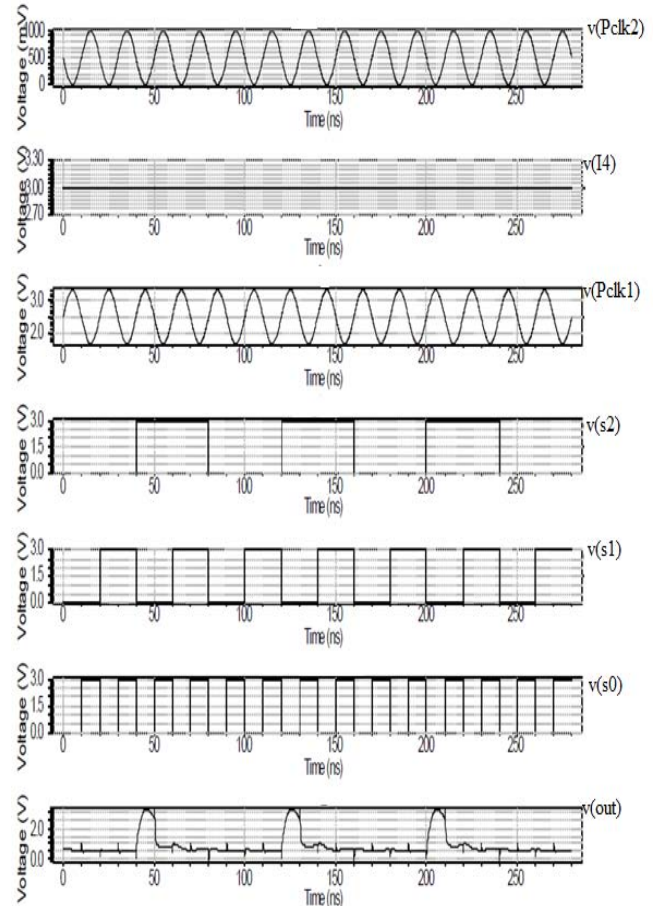the output waveform obtained for the proposed circuit with respect to input I_4 is given in the figure.

Figure 8- simulatiion results of the proposed multiplexer

6. Performance analysis of various logic styles for 8:1 multiplexer

Table 2 shows the power comparison of various logic styles and the proposed 8:1 multiplexer.

TABLE 2

Logic / Parameter	2n2n2p	ECRL	PFAL	Previous circuit Result	Proposed circuit result
Transistor count	68	66	68	66	66
Total power dissipation(μwatts) at 400MHz	54.295	41.721	30.02	16.8	9.9
Total power dissipation(μwatts) at 800 MHz	98.794	83.370	59.849	31.52	14.1

From the table 2, it is clear that the proposed adiabatic multiplexer consumes less power compared with the previously proposed circuit. So this proposed circuit is preferred for the power efficient digital logic circuit designs.

7. Conclusion

This paper has described a simulation of power efficient 8:1 multiplexer based on adiabatic logic. By implementing the adiabatic charging and energy recovery theory, the proposed circuit gives the lowest result in power dissipation of all the simulated adiabatic multiplexers. The power dissipation measurement by TSPICE proved that this approach lowers the power dissipation. The design principle can also be used for designing more complicated adiabatic CMOS circuits and its logic schemes can be a viable candidate for ultra-low energy computing.

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