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Parasitic Capacitance Extraction of 3-D DG-Finfet with Low K Symmetric Spacer Material

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Abstract: ***MOS devices are playing main role key in semiconductor industries. But The future limits on scaling of device is affected on MOS device. FinFET is most proposed device for nano scale industry. This technology is used beyond 50nm technology to reduce Short channel effect in MOS devices. It is designed with non-planner structure. Because of non-planar structure of FinFET parasitic capacitances (Gate oxide capacitance, overlap capacitance and fringe capacitance) makes adverse effect such as lower switching speed of device , making effect on access time, delay and Ion and Ioff of device. In this paper we proposed FinFET methodology to reduce parasitic fringe capacitance and overlap capacitance by optimizing gate side wall with low k dielectric spacer thickness and increase Ion to improve device driving capability. Threshold voltage also having impact of above parameters So device threshold voltage is reduced with low k spacer material i.e at least count of 0.0786v. The poly gate is used for front gate and back gate having work function of 4.65 to controls threshold voltage . Due to high k material leakage current increased but it is maintain using shorted dual gate technology. Our optimization in spacer material results in reducing total gate capacitance (123nF, 131nF and 123nF) and increases turn on time of device. Here 3d 20nm FinFET is design using TCAD tool (Silvaco) with monto Carlo technique.***

Keywords: MOS, FinFET, CMOS, Ion ,Of , Work function, TCAD, TCAD

1. Introduction

MOSFET and CMOS technology is most suitable to design digital electronic circuits. CMOS is very much interactive device for low power applications. It is having higher transconductance factor and power factor as compared to other transistors. MOS and CMOS having satisfactory performances but problem of scaling is occurred. Scaling of device is increased day by day. In VLSI industries device size is shrink and reached up to 20nm. With 20nm device and beyond structure of device is very complex. Distance between source and drain is so small that effect occurred such as short channel effect. FinFET is developed to predict and reduce problems of short channel effect, drain induce barrier lowering e.t.c. After year of 2008 FinFET is likely device in nano industries. Large parasitic capacitance is main problem in FinFET. [1]. Parasitic makes effect on threshold voltage. Because of high parasitic capacitance threshold voltage is also high. Speed of device is directly affected by threshold voltage. As threshold voltage increased device required more time to turn on so tha propagation delay of device also increased [1,8]. To reduce threshold voltage and make device more and more faster parasitic capacitance must reduced.

Parasitic capacitances also having adverse effects on parameters such as On current (Ion), Off current (Ioff) e.t.c. Higher ratio of Ion and Ioff increases speed of device. Higher Ion not only trigger device in short time but also reduce short channel effect [2].Large parasitic capacitance decreases On current of device. Thus purposed different FinFET design technique to improve parasitic capacitances, speed and delay for digital applications.[13]

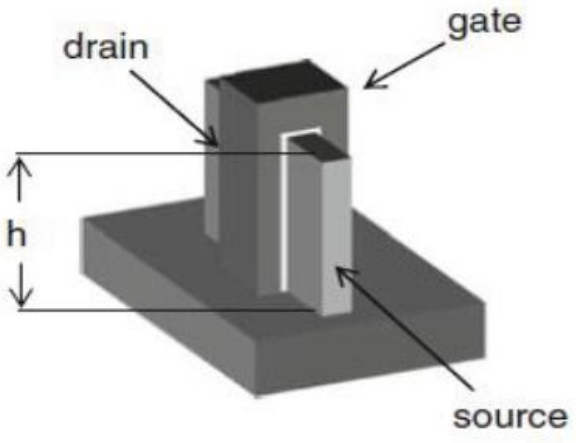

Figure 1(a): shows simple single gate FinFET structure

FinFET is fabricated with different structures such as shorted gate, Independent gate ,all around gate e,t,c.Fig.1(a) shows simple FinFET with single gate. Here tall Fin is fabricated on silicon substrate .Tall Fin increases mobility of device [4]. Fin is wrapped with three sided Gate structure thus having higher control on drain current. But using single gate FinFET structure, device required higher threshold voltage to turn on. To fabricate Drain, source and gate poly silicon material is used. Here gate oxide thickness also affects on threshold voltage. For low threshold voltage, hard mask is used as gate oxide. To improve threshold voltage independent gate structure is proposed[9].

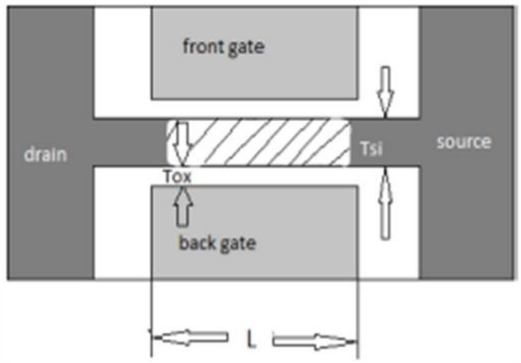

Figure1(b): Shows Dual gate(Front gate – Back gate)FinFET structure

Fig1(b) shows dual gate FinFET having two gates front gate and back gate. Structure of DG Gate and single gate is same only different in structure of gate. Back gate biasing providing low threshold voltage required very small turn on time [2]. Dual gate provide higher Ion to improve speed of device and Short channel effect.

In this paper three types of parasitic capacitances are studied that are gate capacitance which is form due to oxide between gate to substrate. Overlap capacitance which is form due to overlap between drain and gate or source and gate. And finally fringe capacitance is capacitance between two electrode which is not parallel, separated by insulator[1,3,5]. Fringe capacitance increased with high k permittivity dielectric material. High k dielectric material decrease switching speed and delay. In proposed device design FinFET is design with dual low k spacer technique. In this technique The vacant region between gate metal and source/drain region is filled with passivating oxide [5]. Here passivating oxide such as AIR,SIO2 and SI3N4 is used which are low k materials. In this paper symmetric two low k martial is used to reduce these parasitic capacitances. But it increases leakage current of device .Leakage current worsen battery lift. By changing physical characteristic of device, Optimization of device is taken place. Diffusion area makes effect on contact resistance [6].Cross section area and large length of fin increases source to drain resistance than conventional MOS device. Hence increase in FIN peach decrease in gate capacitance and increase in Hfin increase mobility of device [10]. Study of three parasitic capacitances: fringe capacitance [1], [,3], [5] gate capacitance[1] and overlap capacitance[3] taken place and technique is implemented on 20 nm FinFET technology to develop new transistor . N-type FinFET device structure is fabricated using victory device process TCAD simulation and parasitic find through extraction commands.

This paper is organised as follows. In section I.B Effect Of Permittivity, Length And Thickness On Parasitic Capacitances where effect of parasitic capacitance is studied using different characteristics, II Proposed design and Fabrication Procedure where low k spacer DG-FinFET is design with Fabrication procedure and studied its set parameters. Section, III Result and discussion, comparison of different design FinFET is taken place. And finally section IV and V Conclusion and References respectively.

1.1 Effect of Permittivity, Length and Thickness on Parasitic Capacitances

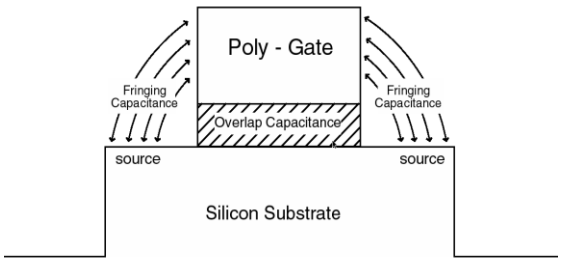

Figure2: Shows different parasitic capacitance of device

Performance of FinFET is govern by Threshold voltage, Ion, Ioff, Gate Capacitance (Cg) Drain Capacitance. And these capacitances depend on permittivity of dielectric material, length and thickness of spacer material. Let see Simple mathematical description of components has been summarised below:

$$C = \varepsilon \frac{L}{D} \quad \text{..... (1)}$$

Where, ε represent the relative permittivity of dielectric material and it is important to change characteristics of capacitances. L represents plate length and d is distance between two plates. In this basic formulae, permittivity is decrease from 3.9 and below and distance between two plates means oxide thickness increase thus parasitic capacitance decrease with respect to ε and D. In this paper study of total gate is analyzed with respective spacer and gate oxide thickness Total gate capacitance is given as

$$Cgtotal=Cox+Cov+Cfr \quad \text{.....(2)}$$

Where

$$Cox = \varepsilon ox(\frac{LgW}{Tox}) \text{ is the oxide capacitance, ...(3)}$$

$$Cov = \varepsilon ox(\frac{LovW}{Tox})$$

is the gate drain overlap capacitance and.....(4)

$$Cfr = \frac{\varepsilon ox}{\alpha} In(1+\frac{tpoly}{tox}) \text{ where } \alpha = \frac{\pi}{2} \text{ is gate side wall fringe capacitance} \quad \text{.....(5)}$$

In eq.5 fringe capacitance is calculated with reference [12]. Fringe capacitance is theoretical calculated by changing material permittivity and Tox.

2. Proposed Design and Fabrication procedure

2.1 Proposed DG FinFET

In This section proposed device design and their parasitic performance has been analyzed through TCAD simulation

tool. Proposed structure inherently effect on parasitic component and FinFET characteristics.

In this paper three type of capacitances is reduced. The structure of optimized dual Gate FinFET is shown in Fig.3(a),Fig.4(a) and fig5(a). The proposed structures having some differences than conventional FinFET w.r.t Structure design. In this DG-FinFET structure symmetric dual k low spacer is implemented to reduce parasitic capacitances. To design the n type FinFET all device parameter is properly selected as shown in table 1.

Table 1: Set Device Parameters

Sr. No	Device Parameter	Symbol	Value(N-FinFET)
1	Fin Height	Hfin	50nm
2	Fin width	Wfin	30nm
3	Fin Length	Lfin	70nm
4	Gate Length	Lg	20nm
5	Gate Height	Hgate	50nm
6	Gate Work function	ϕg	4.65
7	Oxide Thickness	Tox	1.6nm
8	Supply Voltage	Vdd	0.3v
9	Spacer-1 Length	Lsp1	150nm
10	Spacer-1Width	Wsp1	40nm
11	Spacer-1 Thickness	Tsp1	70nm
12	Spacer-2Length	Lsp2	150nm
13	Spacer-2Width	Wsp2	20nm
14	Spacer-2 Thickness	Tsp2	70nm

2.2 Fabrication Procedure

Fig 3 (a) shows 3D DG FinFET device having two symmetric spacer with different permittivity materials. Here bulk silicon is taken as substrate at orientation of(110). Here device is fabricated with different spacer materials on same substrate wafer. Next vertical tall fin is fabricated with electron beam lithography. Device channel is form in parallel to (110) direction with active masking and etching process. Thickness of fin is 50nm which increases mobility of device. Here Dual gate structure is fabricated with SI3N4 as gate oxide. Gate oxide is form using selective etching process with thickness of 1.6nm. Then parallel to drain and source terminals two spacer is form having symmetric to each other with thickness of 70nm.

Next contacts are form with poly silicon and geometrically etch is performed to remove unwanted material from contacts. After gate and spacer designing, impanation process is started. first boron having dose of 1e13 is deposited with tilt0 ion implantation. Then barrier is deposited to protect channel from implantation of arsenic doses on channel. Then arsenic dose is imposed on device with concentration of 2e14. After ion implementation, thermal annealing performed at 1024 oC temperature for 2second to active impurities when device biased. So that device having higher conductivity and large number of ions are deposited on device. After ion implantation, barrier on top of device is removed by geometric etching. Thus barrier area is used to protect channel. Next electrode of device is implied to provide biasing of device.

2.3 Dual Gate FinFet with SI3N4-SIO2 low k spacer

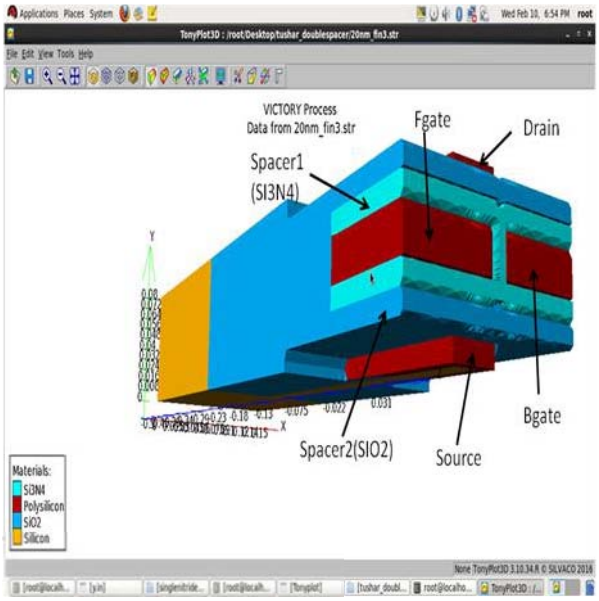

Figure 3 (a): The 3-D view of structure of double gate FinFet with low k spacer(SI3N4+SIO2)

As per shown in Fig.3(a) with two different materials having low permittivity dielectric constant is used. First high k-material (SI3N4) used having permittivity of 7.5 and second material SIO2 having permittivity of 3.9. Both materials are symmetric and gate oxide as SI3N4 is used. Fin is sufficient large so that mobility of device is increased.

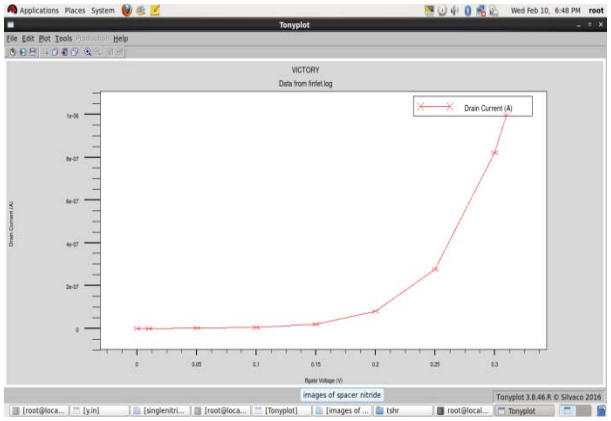

Figure 3(b): shows IV characteristic of FinFET with threshold voltage (vth)=0.1589v

Fig 3(b). shows IV characteristic of designed double low k spacer FinFET having very low threshold voltage which is 0.1589v to trigger device. Device is saturated at 0.3v.Spacer material also effects on threshold voltage. Low k material having very low threshold voltage as compared to high k material. Hence speed of device also improved which mostly advantageous for digital applications such as SRAM.

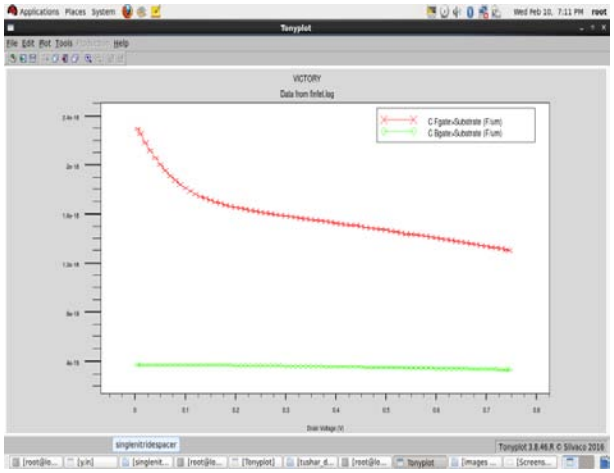

Figure 3(c): shows gate capacitance with spacer(SI3N4+SIO2)

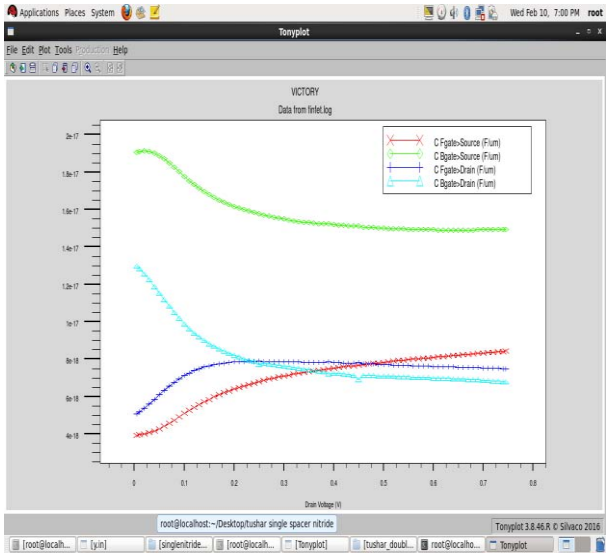

Figure 3(d): shows overlap capacitance with spacer(SI3N4+SIO2)

Above fig3(c) Shows effect of oxide material on gate capacitance. To increase driving capability of device gate oxide must be thinner for short channel up to 20nm. Hence SI3N4 is used as gate oxide. Due to high k material with thin layer leakage current is also reduced. Here fgate–substrate oxide capacitance is higher as compared to Bgate-substrate oxide capacitance. Overlap is basic building block of parasitic capacitance in small scale device. To increase speed of device and reduce overlap capacitance overlap between gate-drain and gate-source should be minimum. For that spacer technique is used with low k material. Low k material effects on charging and discharging of capacitance hence device parasitic is reduced. As compared with above two characteristics as shown in fig3(d) the effect of low k permittivity material on device capacitance. Increase in spacer length reduction in overlap capacitance of device.

Here overlap capacitance Fgate-source and Bgate-source is very much smaller as compared to Fgate-drain and Bgate-drain.

2.4 Dual Gate FinFet with SI3N4+AIR low k spacer

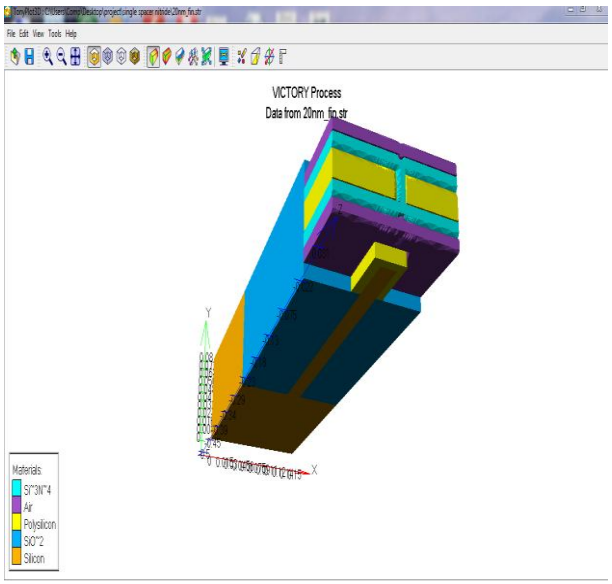

Figure 4(a): The 3-D view of structure of double gate FinFet with low k spacer(SI3N4+AIR)

As per shown in Fig.4(a) with two different materials having high k and low k permittivity dielectric constant is used. First material (SI3N4) used having permittivity of 7.5 and second material AIR having permittivity of 1. Both material used are symmetric. Second material is AIR which is very low k material provides low parasitic capacitance effect rather than previous method used. Because of used AIR as dielectric, permittivity is very low thus problem of leakage current is increased in some range but capacitance reduce drastically.

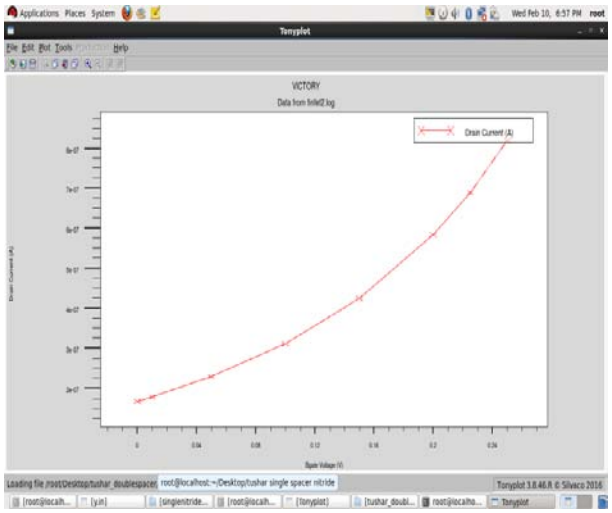

Figure 4(b): shows IV characteristic of FinFET with threshold voltage(vth)=0.0959v

Fig 4(b). shows IV characteristic of designed spacer device(SI3N4-AIR) FinFET having very low threshold voltage which is 0.0959v to trigger device as compared to spacer device(SI3N4-SIO2). Device is saturated at 0.24v.Effect of spacer also seen on threshold voltage. For high k and very low k spacer device having very small threshold voltage so that device trigger in short time.

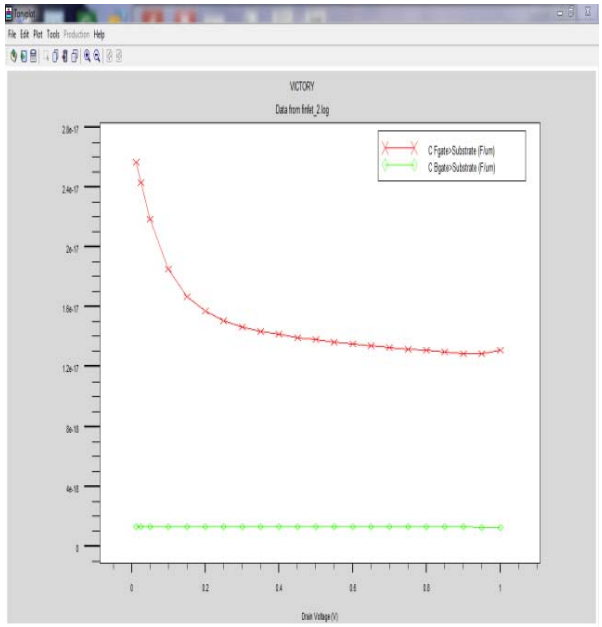

Figure 4(c): shows gate capacitance with spacer(SI3N4+AIR)

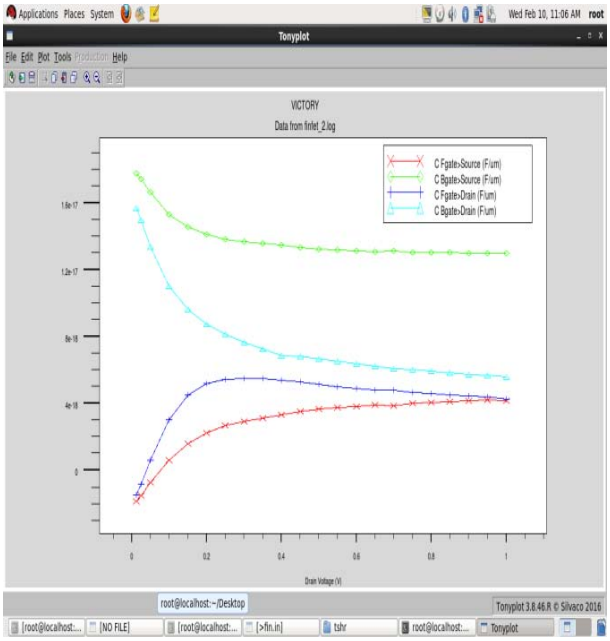

Figure 4(d): shows overlap capacitance with spacer(SI3N4+AIR)

Above fig4(c) Shows effect of oxide material on gate capacitance. As compared to SI3N4-SIO2 spacer device this device having higher Fgate-substrate capacitance. Thus controllability of device is increased. This effect helps to reduce leakage current of device.

Fig4(d). Shows effect of SI3N4-AIR spacer device on overlap capacitance .Overlap capacitance is drastically decreased with used of very low k material. Overlap capacitance of SI3N4-SIO2 device is much more larger than SI3N4-AIR.Both capacitance i.e both gates-drain and both gates-source is reduced which is much more beneficial.

2.5 Dual Gate FinFET with SIO2+AIR low k spacer

This is most proposed structure having very small parasitic capacitance as compared to above both. As per shown in Fig.5(a) with two different materials having low permittivity dielectric constant is used. First material (SIO2) used having permittivity of 3.9 and second material AIR having permittivity of 1. Both low k material used are symmetric. Here permittivity of SIO2 is smaller than SI3N4 hence parasitic capacitance is smaller than both above device designed.

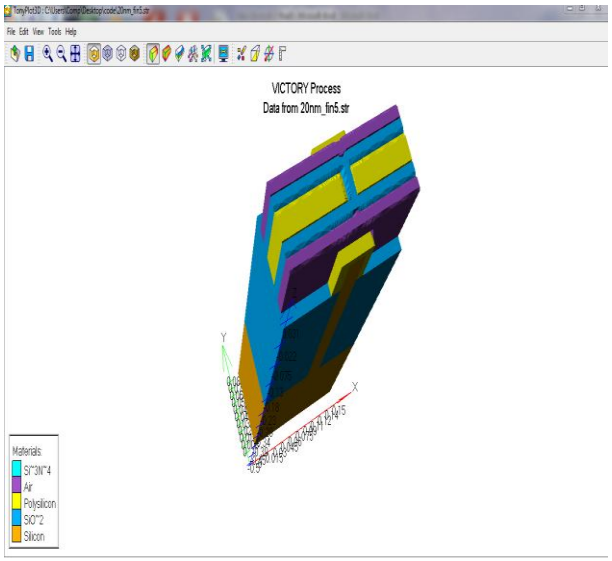

Figure 5(a): The 3-D view of structure of double gate FinFet with low k spacer(SIO2+AIR)

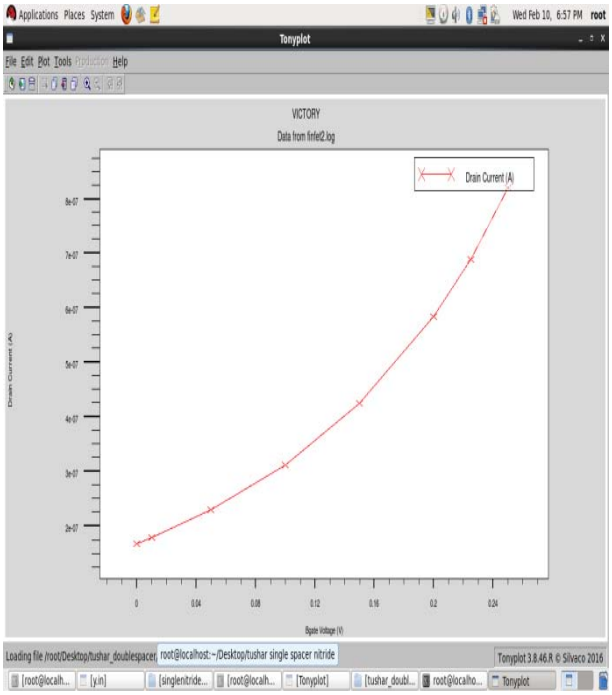

Figure 5(b): shows IV characteristic of FinFET with threshold voltage(vth)= 0.07856v

Fig5(b). shows IV characteristic of designed spacer device(SIO2-AIR) FinFET having least threshold voltage which is 0.0785v to trigger device as compared to spacer device(SI3N4-SIO2) and(SI3N4-AIR). Device is saturated at

0.24v.Effect of spacer also seen on threshold voltage. For very low k spacer device having very small threshold voltage so that device trigger in short time and required very small access time. In this paper this device having almost least parasitic capacitances and mainly approach to use in SRAM design.

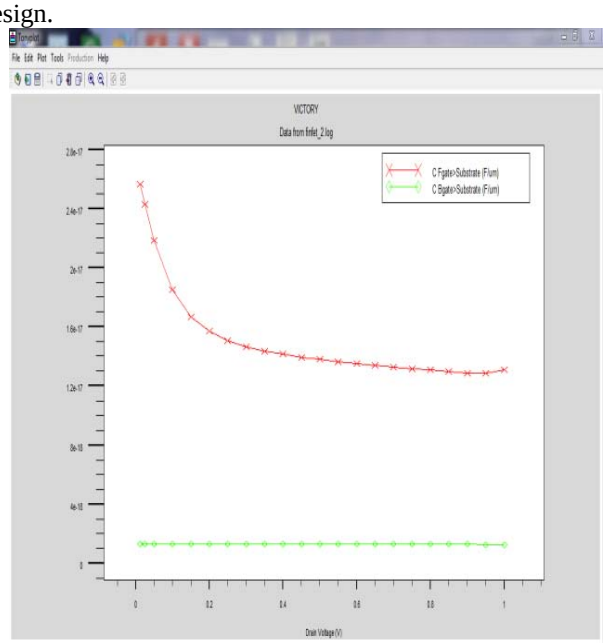

Figure 5(c): shows gate capacitance with spacer(SIO2+AIR)

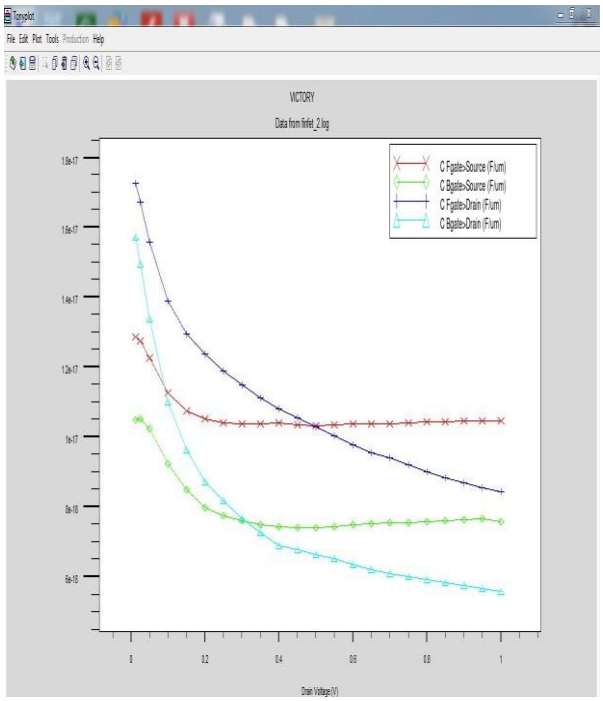

Figure 5(d): shows overlap capacitance with spacer(SIO2+AIR)

Above fig5(c) Shows effect of oxide material on gate capacitance. Oxide capacitance of SIO2-AIR spacer device having same characteristic as compared with SI3N4-AIR spacer device.

Fig5(d). Shows effect of SIO2-AIR spacer device on overlap capacitance .Overlap capacitance is drastically decreased with used of very low k material. Overlap capacitance of SI3N4-SIO2 and SIO2-AIR device is much more larger than SIO2-AIRspacer device. Both gates-drain and both gates-source is reduced which is required for high speed SRAM.

2.6 Impact of Fringe Capacitance.

Fringe capacitance is parasitic capacitance which is occurred at corner of device. Effect of fringe capacitance is dependent on dielectric material. Performance of device is decrease because of high dielectric.

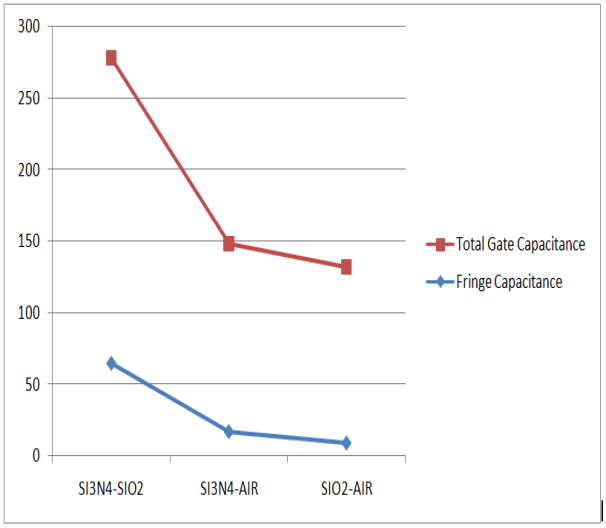

Figure 6: shows fringe capacitance and total gate capacitance

Here in fig.6 shows drastically changes in total gate capacitance because of fringe capacitance. There are two types of fringe capacitance first inner fringe capacitance and second outer fringe capacitance. In this paper inner fringe capacitance is studied. Here impact of SI3N4,SIO2and AIR on fringe components are studied. Total gate capacitance very much higher than fringe capacitance. As shown in figure Impact of fringe is very much higher in SI3N4-SIO2 spacer structure and vise versa for SIO2-Air Spacer structure.

For digital application the device performance is dependent on delay which is rate of change of Ion. And Ion is affected by fringe capacitance. So that Ion/off ratio must be high for high speed digital application.

3. Result and discussion

Table 2: Shows comparison of gate capacitance between (SI3N4+AIR) and (SI3N4+SIO2) Spacers

Sr. No	Parasitic capacitance	Dual spacer(Oxide+Air)	Dual spacer (Nitride+Air)	Dual spacer (Nitride+ Oxide)
1	fgate-sub	1.567e-17	1.31e-17	1.3055e-18
2	bgate-sub	1.9852e-18	1.28e-18	3.3e-19

Table 3:.shows comparison of Overlap capacitance between (SI3N4+AIR) and (SI3N4+SIO2) Spacers

Sr. No	Parasitic capacitance	Dual spacer (Oxide+Air)	Dual spacer (Nitride+Air)	Dual spacer (Nitride+Oxide)
1	fgate-source	3.2545e-18	3.9727e-18	8.426e-18
2	bgate-source	1.2259e-17	1.3e-17	1.302e-17
3	fgate-drain	3.547e-18	4.644e-18	7.47e-18
4	bgate-drain	2.4587e-18	5.5732e-18	6.784e-18

Table no. 2 shows comparison of gate capacitance with different spacer technique. Here gate capacitance is increased because SI3N4 is used as gate oxide. Main reason behind using SI3N4 as gate oxide is that it having higher permittivity than SIO2 thus at thinner layer driving capability of device is increased. So that at thinner layer problem of tunnelling is not occurred.

Table no 3 shows overlap capacitance. Overlap capacitance form because of amount of area which is in between gate to drain and gate to source. With low k permittivity material overlap capacitance is decreased. Here with SIO2-AIR spacer device having least overlap capacitance.

4. Conclusion

Double gate with low k spacer material is designed to reduce parasitic capacitance i.e total gate capacitance. Here FinFET designed and analyzed on 20nm technology with silvaco tcad tool. High k material makes adverse effect on parasitic capacitance. MOS devices are affected by scaling of technology because of short channel effect and higher parasitic capacitance. Thus results in large threshold voltage to turn on device. Threshold voltage is affected by different material such as high k(SI3N4)material, low k(SIO2)material and very low k(Air)material. With passivating oxide as AIR is mostly used to reduce threshold voltage. In this paper threshold voltage is very low i.e 0.7856v. In this paper we proposed dual gate low k spacer technique for FinFET design to reduce parasitic capacitances and improve threshold voltage to enhance speed of device In this approach symmetric spacer thickness with two different material is used to improve performance of device. The proposed technique also improved Ion of device. Device Ion current improves speed, driving capability and short channel effect. Hence it is proved that using low k spacer technique with different material minimize effect of parasitic very efficiently. In future low k material (Florin, Teflon e.t.c) implantation will be advantageous for parasitic capacitance reduction and making less trade of between speed of device and leakage current

5. Acknowledgment

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