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Design and Analysis of Low Power High Speed Hybrid Alternative Full Adder Circuits

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Abstract: ***These This project deals designs of 1-bit hybrid alternative full adder using complementary metal-oxide-semiconductor (CMOS) logic, gate diffusion input (GDI) technique, modified GDI and transmission gate logic are reported. These designs are implemented using Mentor graphics tool. Performance parameters such as power dissipation and transistor counts are compared with other designs and the existing designs such as complementary pass-transistor logic, transmission gate adder and hybrid pass-logic with static CMOS output drive full adder, transmission function adder, mixed topology of GDI with both inverter and mirror so on. This design is divided into three modules and found to working efficiently with less power dissipation and transistor count at 180nm technology.***

Keywords: CMOS, hybrid adder, GDI full adder, low power, transistor count and adders

1. Introduction

The most important feature of current electronics is low power and energy efficient which are the major elements that give the ability in carrying out long operated battery life systems. As there is an improvement in the technology, there is an increased demand for the battery operated devices which is leading to the exponential growth of the electronic portable devices. Low energy operations are very important for deep- sub micron technologies and to improve the battery life of the system. The goal of VLSI (Very Large Scale Integration) design in low power nano electronics technology is to achieve high performance parameters such as power consumption, delay and power delay product.

The battery technology does not have the same enhancement as that of micro- electronic technology there is no sufficient amount of power as required by the mobile systems. So the designers are facing problem with some constraints, like high speed, high throughput, smaller silicon area and low power consumption. So constructing low power high efficient adder cells is of greater interest [8]. Addition is the main arithmetic operation and is used in many VLSI systems.

2. Design Approach of the Proposed Full Adder

2.1 Full adder circuits

Full adder is a logic circuit. These adders placed inside in the form of arithmetic logic unit in recent computers, where other operations are performed. This adder shows an addition operation on three one bit binary numbers and produces a sum and a carry. Figure 1 shows the basic block diagram of full adder. It has one bit of three binary inputs and two binary outputs.

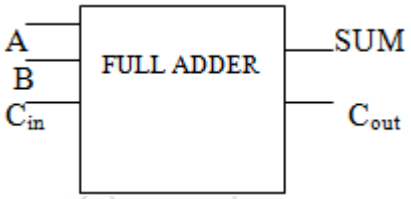

Figure 1: Basic block diagram of full adder

The binary adder design is start by assuming the process of summation in base 2, as shown in figure 2.

$$\begin{array}{r} 111 \\ 1001 \\ +0111 \\ \hline 10000 \end{array} \quad + \quad \begin{array}{r} 9 \\ 7 \\ \hline 16 \end{array}$$

Figure 2: 4-bit binary addition sample problem

From above example the two binary numbers are added like 1001+0111, are written in the form of one above the other. The carries are written above them and it is shifted from one column to next. Final answer is in the form of 5-bit number 10000. This adder sum is match to the decimal addition like 9+7=16. Here declare that the problem of adding two 4-bit binary numbers can be optimized to the problem of adding a column of two or three bits and carry moved to the next column. This binary addition said that adding of column vice (bit by bit) of binary values to get sum and carry output in above example as well as decimal result also.

In the digital arithmetic circuits, binary adder is a necessary building block. Its plan is to generate the arithmetic sum and carry of two digital numbers. It performs an addition operation on three binary inputs such as A, B and C and produces a sum and C_{out} output values. Then Boolean equations and truth table as shown in below table 1.

$$\text{Sum} = A \text{ XOR } B \text{ XOR } C_{in} \quad (1)$$

$$C_{out} = (A \text{ AND } B) \text{ OR } (B \text{ AND } C_{in}) \text{ OR } (C_{in} \text{ AND } A) \quad (2)$$

The cascading of two half adder is used to construct a full adder. The input of the first half adder is the A and B are connected and the sum of first half adder is connected as one input along with C to second half adder and it produce sum output shown in equation (1) . The logical OR of first and second half adder carry output a gives C_{out} of full adder shown in equation (2).

Table 1: Truth table for full adder

A	B	C	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.2 The1-bit hybrid full adder structures

A hybrid full-adder operation is composed of a CMOS logic, transmission logic gate and GDI full adder. This hybrid full adder is divided into three modules as shown in figure 3. Module 1 and module 2 are the XOR modules that generate the sum signal (SUM) and module 3 is generates the output carry signal (*Cout*). Each module is designed use different logic style.

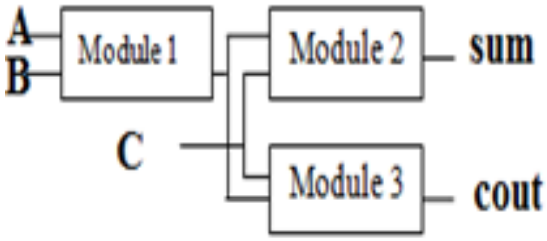

Figure 3: Schematic structure of full adder

Figure 4 is the logic circuit of full adder. It is drawn by using Boolean expressions are obtained by the making a truth table listing the outputs for all possible combination of inputs. Logic circuits can be designed based on expressions.

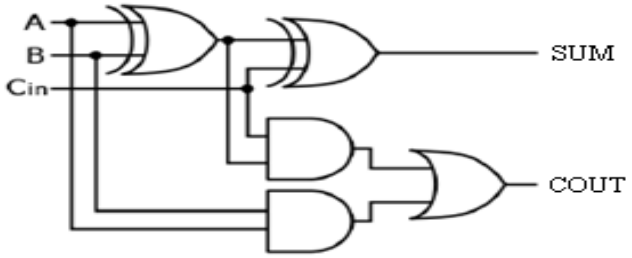

Figure 4: Logic circuit of full adder

3. Design Implementation and Operation of the proposed Hybrid Full Adders

Proposed hybrid alternative full adder schematic structures and designs are follows below

3.1 Hybrid full adder design 1

Figure 5 shows the schematic design structure of hybrid adder 1 contains two different logic design styles combined together to form high performance parameters. For low power dissipation and high speed operation of cross-coupled PMOS pull up and NMOS pull down devices providing the CMOS logic of sum output. The optimized transistor counts of GDI technique for C_{out} generation. This hybrid adder design gives overall performance of full swing output.

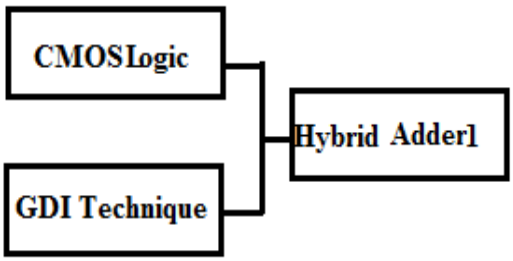

Figure 5: Schematic design structure of hybrid adder design 1

Figure 6 shows the schematic detailed diagram of the proposed hybrid full adder. It consists of 30 transistors to generate whole 1-bit hybrid adder. Module 1 and 2 are XOR-XOR circuit designed using CMOS logic generates sum output with full swing. Module 3 is constructed using multiplexer circuit is designed with gate diffusion input (GDI) technique. It requires less number of transistors are provides C_{out} output signal. This circuit design provides excellent performance parameter in terms of power consumption transistor counts. Because CMOS logic consumption very less power to operate the function.

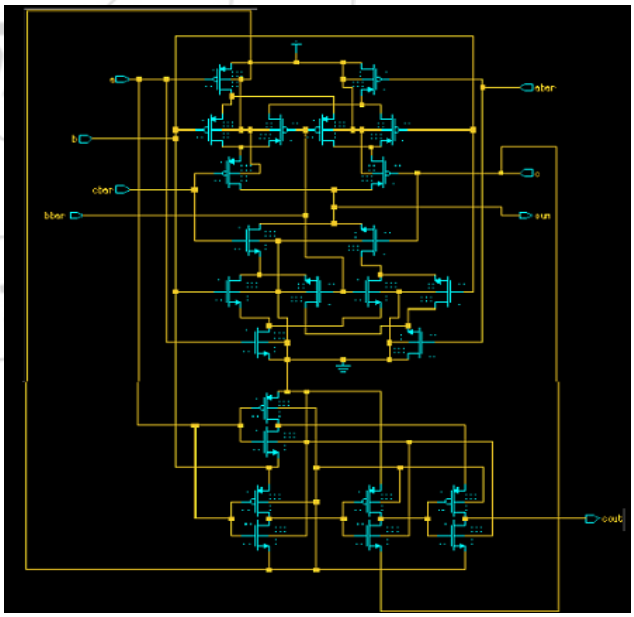

Figure 6: Proposed schematic diagram of 1-bit hybrid full adder design 1

3.2 Hybrid full adder design 2

Figure 7 shows the structure of hybrid adder 2 and composed of two different logic design styles like transmission gate logic and GDI technique to provide good performance as compared to other full adders and some hybrid adders. Sum output of

this circuit is designed using GDI technique and has better performance in terms of number of transistor counts to use and low power dissipation compare to other GDI full adders. Transmission gate logic is a parallel arrangement of PMOS and NMOS devices used for designing a C_{out} signal. Hence we are using alternative hybrid adder design styles to improve the performance of VLSI circuits.

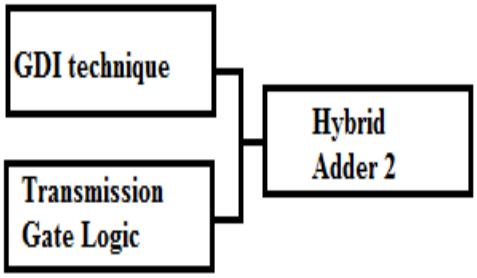

Figure 7: Schematic design structure of hybrid adder design 2

Figure 8 shows the schematic diagram of alternative proposed full adder circuit 2.

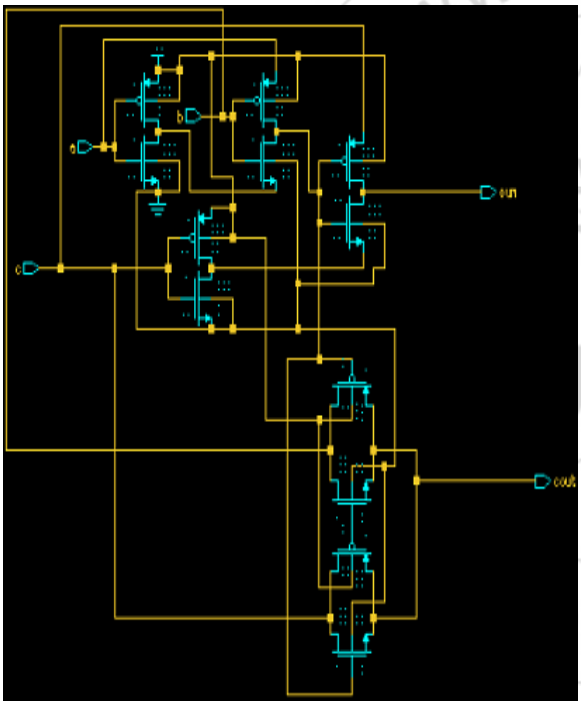

Figure 8: Proposed schematic diagram of 1-bit hybrid full adder design 2

The design consists of GDI property for sum output generation and transmission logic gate for carry output generation. This hybrid adder consists of 12 transistors. Module 1 and 2 are XOR-XOR circuit is used to design GDI technique provides sum full swing output. This design is lowest power dissipation design technique. Using only two transistors for this design can build many varieties of logic functions. This circuit design using optimized number of transistors (as compared to CMOS and TG full adder), while increasing logic level swing. Module 3 are multiplexer circuit is designed using transmission gate logic in the form of parallel arrangement of PMOS and NMOS transistors generates C_{out} signal. It gives high speed improvement is degraded some time due to the threshold loss and driving capability of transmission gate circuit design.

3.3 Modified hybrid full adder design 1

The modified hybrid 1-bit full adder design 1 is shown in figure 9. To study the different performance parameters of the adders a structural design of a hybrid full adder is modified GDI by optimizing power consumption in XOR circuit because XOR module is supervise for most of the power consumption of the overall sum output of the adder circuit.

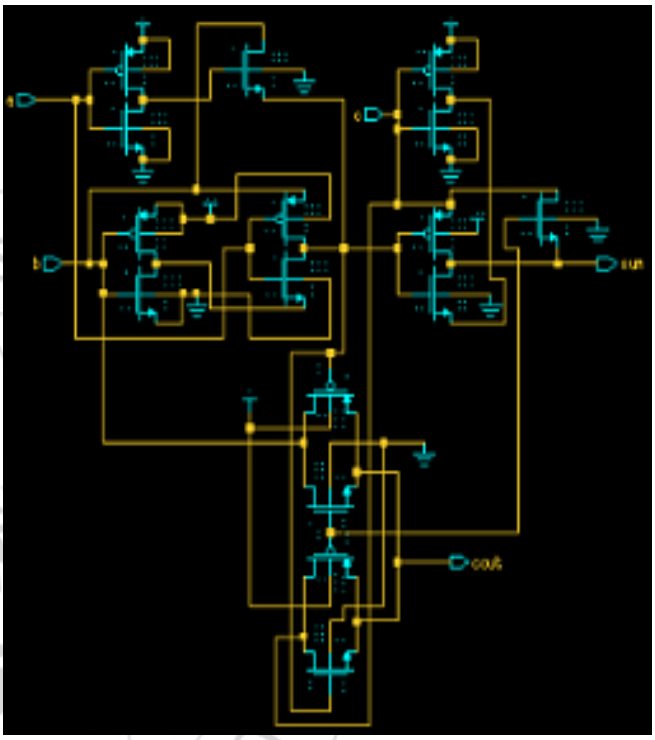

Figure 9: Modified hybrid adder design 1

3.4 Modified hybrid full adder design 2

Figure 10 shows the detailed diagram of the proposed modified hybrid full adder design 2.

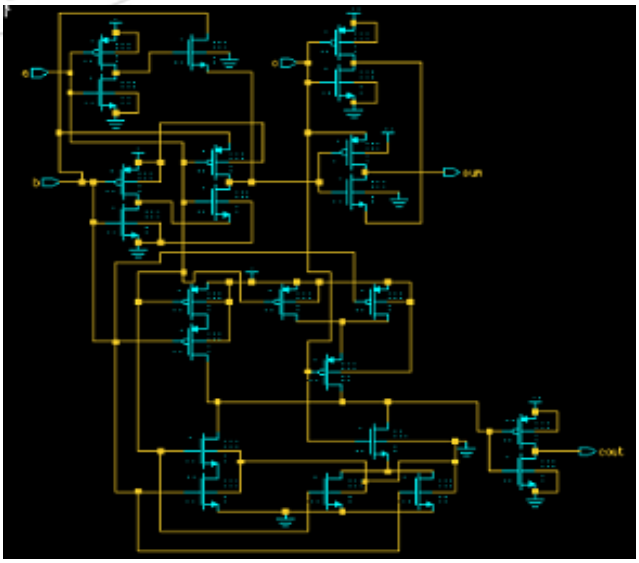

Figure 10: Modified hybrid adder design 2

The GDI technique has less transistor counts to design a circuit and then it is modified for full swing output and better performance at medium supply voltage (1.8V).

3.5 Modified hybrid full adder design 3

Figure 11 shows the proposed schematic diagram of modified hybrid adder 3 and its design consists of three modules. Module 1 and module 2 are the XOR circuit designed with CMOS logic and module 3 are the multiplexer are designed with Modified GDI technique together to generates sum and carry outputs of the overall hybrid full adder. This design consists of 34 transistors to obtain whole 1-bit hybrid adder. The power consumption is less compared with other design styles of the hybrid and modified hybrid adders.

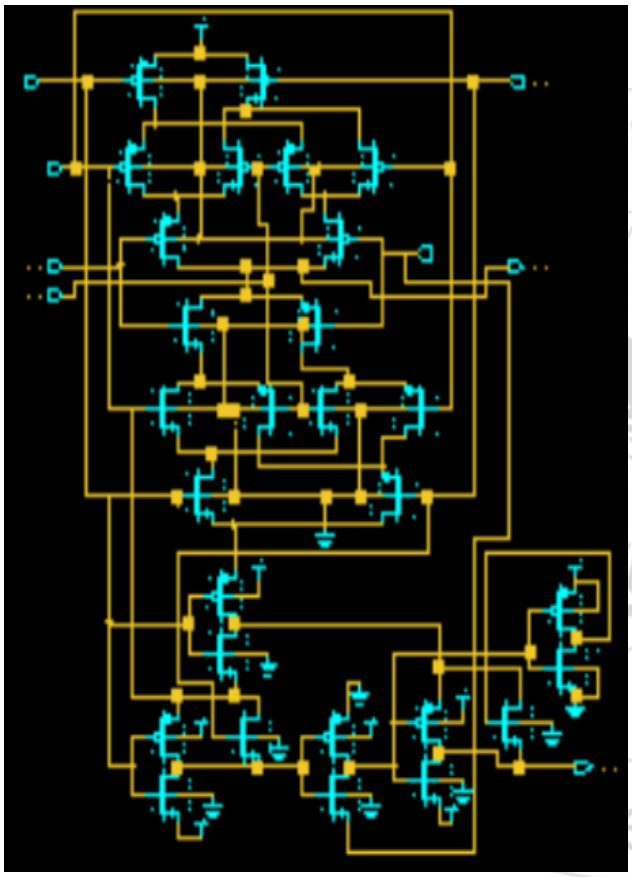

Figure 11: Modified hybrid adder design 3

4. Analysis and Simulation Results

The proposed hybrid adder simulations was carried out in mentor graphics tool with 180nm technology and compared with the other potential hybrid adder circuit designs reported in table 2. The main aim of this project is to improve the power consumption could be reduced by using GDI technique and CMOS logic. It was observed in the current circuit designs. The proposed hybrid adder cells have been 30-T, 12-T, 16-T, 23-T and 34-T transistors significantly. The proposed hybrid design 1 and modified hybrid adder design 3 has lower power consumption than that of other hybrid full adders. But modified hybrid adder design 3 has been require more number of transistors to design. For that purpose hybrid adder design 1 is better power dissipation compared to other hybrid adders. The use of less number of transistors realizes the hybrid adder designs 2 is improved the speed.

Table 2: Comparison between simulation results of different hybrid full adders in 180nm technology

Types of Hybrid Adders	Power Consumption (µw)	Transistor Counts
Hybrid Full Adder (180/90nm)	4.1563/1.17664	16-T
Hybrid Full Adder (90nm)	0.20711	16-T
Hybrid Full Adder Cell (180nm)	0.318	26-T
Hybrid Full Adder (180nm)	3.007	14-T
Proposed Hybrid Adder Design 1	0.0037692	30-T
Proposed Hybrid Adder Design 2	8329800.0	12-T
Proposed Modified Hybrid Adder Design 1	2495400.0	16-T
Proposed Modified Hybrid Adder Design 2	2495200.0	23-T
Proposed Modified Hybrid Adder Design 3	0.0071517	34-T

Simulations output waveforms of hybrid adder designs provided the sum and carry output values using different input pattern and provide different performance parameters as shown below.

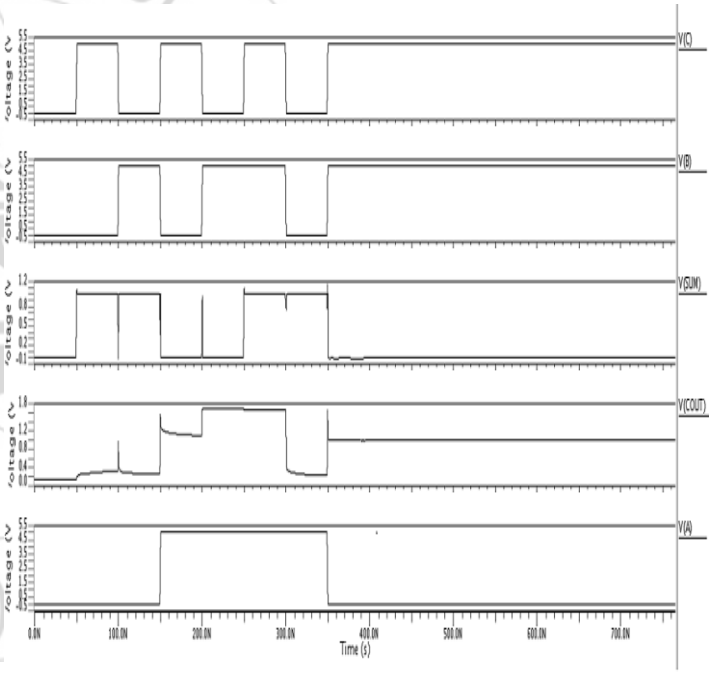

Figure 12: Simulation waveform of hybrid adder design 1

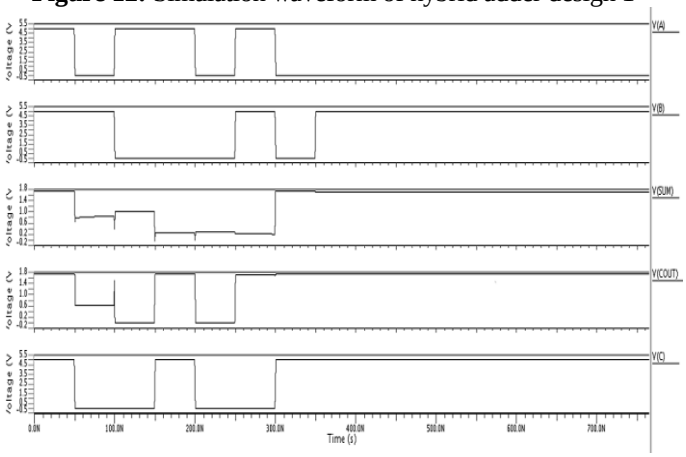

Figure 13: Simulation waveform of hybrid adder design 2

Simulation waveform and power dissipation results of modified hybrid full adders as shows below

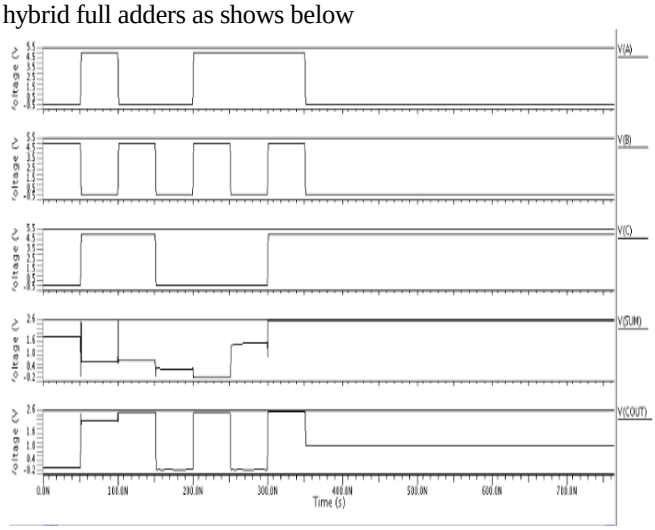

Figure 14: Simulation waveform of modified hybrid adder design 1

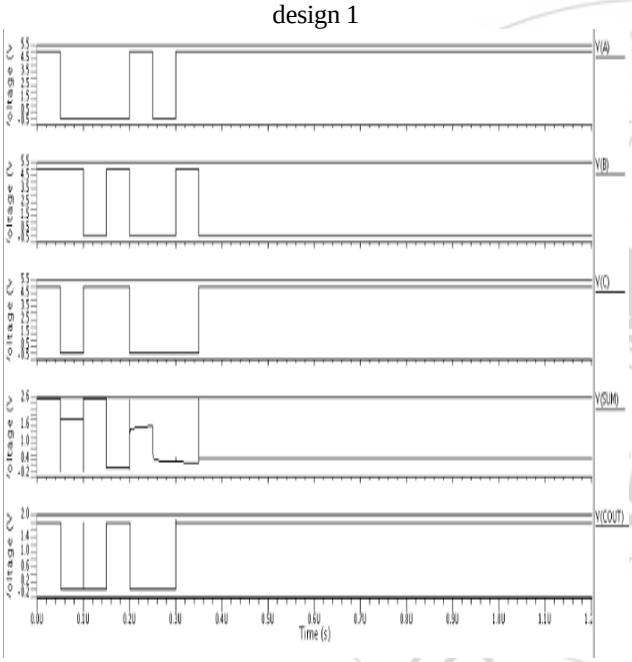

Figure 15: Simulation waveform of modified hybrid adder design 2

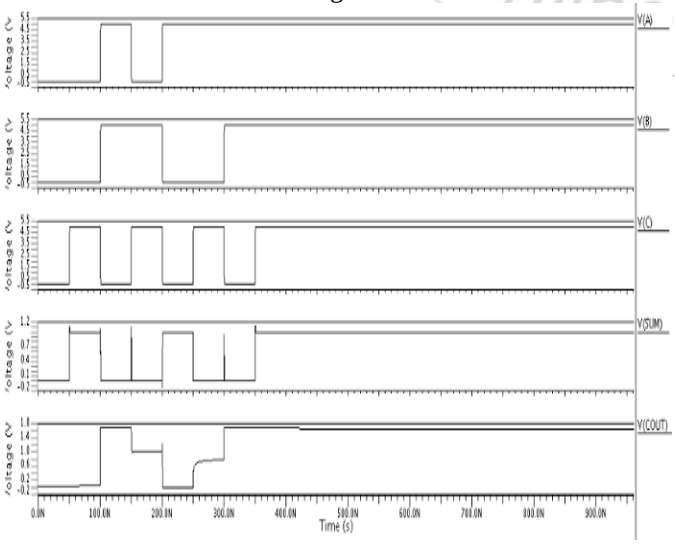

Figure 16: Simulation waveform of modified hybrid adder design 3

5. Conclusion

In this paper, low power 1-bit hybrid full adder circuits using alternative design styles has been proposed and first two designs like hybrid adder 1 and 2 are extended to 2-bit also. The simulation was successfully implemented in mentor graphic tool with 180nm technologies and compared with other standard design approaches like CPL, TFA, TGA, CMOS and other hybrid adder designs. Power dissipation is least in the case of transmission gate and Gate diffusion input technique transistor implementation of hybrid full adder. Simulation result of proposed hybrid adder design 1 provided the improved power dissipation compared with earlier hybrid adder reports and hybrid Adder design 2 is better in terms of number of transistors used to realize the adder.

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