

Hardware ECG QRS Complex Detector in Low Power SoCs

Minh D. Nguyen¹, Giang V. Nguyen²

^{1,2}School of Electronics and Telecommunications, Hanoi University of Science and Technology, Hanoi, Vietnam

Abstract: *This paper proposes a new hardware architecture implementing a low cost, energy efficient electrocardiograph (ECG) QRS complex detector. The proposed architecture can be used as an accelerator in an ultralow power System on Chip (SoC) which is the most important part of ECG devices. The architecture implements the modified version of MaMeMi filter algorithm [1]. The architecture is validated using the MIT-BIH Arrhythmia databases. More than 98.8% of all QRS complexes were detected correctly by the architecture. The architecture is synthesized using 45nm CMOS technology and occupies the area of 0.23 mm² and dissipates the total power of 1.26mW.*

Keywords: Hardware, ECG, QRS, SoC, low power

1. Introduction

According to World Health Organization, cardiovascular diseases are the major cause of death worldwide. Electrocardiogram (ECG) analysis is the useful, inexpensive, common screening tool for a variety of cardiac abnormalities. However, to perform ECG analysis, the patients need to visit a professional clinic to be monitored in a short period of time only. Patients can also carry Holter devices that collect ECG data in a long period of time (from 24 hours to 2 weeks). Holter devices collect ECG data during patient daily activities which helps cardiovascular physicians diagnose heart-related diseases better. However, Holter devices are not real-time monitor devices and are not able to warn the hospital/doctor/patient immediately when a critical heart abnormality occurs. Recently, thanks to technology advances, wearable, battery-operated devices are introduced to replace the traditional ECG monitors. These devices can be comfortably carried by the patients that automatically collect ECG data and monitor/detect heart abnormalities in real-time for a long period. Currently, researchers have been focusing on developing energy efficient ECG devices in both software and hardware levels.

In software level, many algorithms were proposed. A comprehensive survey on QRS Detection Methodologies for Portable, Wearable, Battery-Operated, and Wireless ECG Systems is reported in [Error! Reference source not found.]. In [Error! Reference source not found.], authors compared many algorithms in term of noise robustness, numerical efficiency. These algorithms are partitioned into two phases: QRS enhancement and QRS detection which were compared separately. In [Error! Reference source not found.], Gradl et.al. developed an Android application that monitors ECG in real-time and is able to detect arrhythmia automatically. A simple real-time QRS detector based on MaMeMi filter was proposed. MaMeMi filter is non-linear filter based on moving maximum and minimum functions.

In hardware level, researchers proposed to implement QRS hardware detectors using Hardware Description Language

(HDL) [Error! Reference source not found., Error! Reference source not found., Error! Reference source not found.]. In [Error! Reference source not found.], a pattern recognition algorithm is implemented using Verilog Hardware Description Language (HDL) and synthesized by Xilinx software. In [Error! Reference source not found., Error! Reference source not found.], mathematical morphological method is implemented to removed baseline wandering and background noises. The proposed hardware is synthesized into nano-FPGAs to validate their resource usages (in term of chip area and power consumption). Recently, several SoC architectures are proposed as a the most important parts of ECG sensor nodes in Body Area Network (BAN) [Error! Reference source not found., Error! Reference source not found., Error! Reference source not found.]. In proposed SoCs, the heart beat detector was usually implemented as a separate hardware accelerator in order to reduce chip power consumptions.

In this paper, we propose a new hardware architecture for the hardware QRS detector. The detector will be used in SoC ECG sensor node as an accelerator. The architecture implement a very simple QRS detection algorithm. The paper is organized as follows. In Section II, the QRS detection algorithm is briefly described. Section III proposes the hardware architecture implement the QRS detection algorithm. In Section IV, the experimental results are shown to demonstrate the efficiency of the proposed hardware. Section V concludes the paper.

2. QRS detection algorithm

QRS events are the most important part of ECG signal. By detecting QRS events, the other events as P and T wave can be detected. Also, heart beats are inferred by measure the period between R peaks in the detected QRSs. However, detection of QRSs is not simple as ECG signals are affected by different sources of noises, heart abnormal activities,... Researchers has been intensively investigating in QRS detection algorithms for past two decades. However, recently, lightweight algorithms attracted the interest of the

research community as low power consumption requirement of ECG sensors. In this section, we propose a modified version of the MaMeMi algorithm [Error! Reference source not found.]. The algorithm can be described using Figure 1.

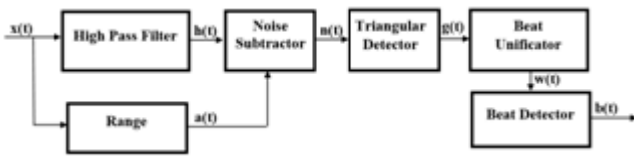


Figure 1: MaMeMi-based QRS detection algorithm

In order to detect QRS complexes, first ECG signals should be enhanced by filtering the low and high frequency noises from the signals. In order to reduce the algorithm complexity, the MaMeMi method uses a high pass non-linear filter based on maximum, mean and minimum values of ECG signals. [Error! Reference source not found.]. The MaMeMi output is defined as:

$$h(t) = x(t) - \frac{\max^*(t) - \min^*(t)}{2} \quad (1)$$

$$\max^*(t) = \begin{cases} x(t) & \text{if } t = 0 \\ \max^*(t-1) + \Delta \cdot \sigma & \text{if } x(t) > \max^*(t-1) \\ \max^*(t-1) - \Delta & \text{if } x(t) \leq \max^*(t-1) \end{cases} \quad (2)$$

$$\min^*(t) = \begin{cases} x(t) & \text{if } t = 0 \\ \min^*(t-1) - \Delta \cdot \sigma & \text{if } x(t) < \min^*(t-1) \\ \min^*(t-1) + \Delta & \text{if } x(t) \geq \min^*(t-1) \end{cases} \quad (3)$$

Where $x(t)$ is the ECG input signal, $\max^*(t)$ and $\min^*(t)$ are the delayed versions of the maximum and the minimum of $x(t)$, respectively. In the equation, the algorithm parameters Δ and σ determined the speed of the maximum and minimum to follow the input signal $x(t)$.

From $\max^*(t)$ and $\min^*(t)$, the pseudo high frequency noise $a(t)$ is deduced:

$$a(t) = \max^*(t) - \min^*(t) \quad (4)$$

Then, the high frequency noise is subtracted from the signal:

$$n(t) = \begin{cases} \text{sign}(h(t)) \cdot (|h(t)| - a(t)) & \text{if } a(t) \leq h(t) \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

The enhanced signal $n(t)$ is then filtered using triangular detector to reduce the QRS pulse width. The triangular detector is based on Eq. 6, where β is the half of the distance between two QRS peaks which is chosen to be 15.

$$g(t) = \begin{cases} n(t) - \max(n(t-\beta), n(t+\beta)) & \text{if } n(t) > 0 / n(t-\beta) < n(t) > n(t+\beta) \\ n(t) + \min(n(t-\beta), n(t+\beta)) & \text{if } n(t) < 0 / n(t-\beta) > n(t) < n(t+\beta) \\ 0 & \text{otherwise} \end{cases} \quad (6)$$

After that, heart beat is identified by using an adaptive threshold algorithm as shown in Figure 2. In the algorithm, heart beats are defined as signal peaks which are greater than an adaptive threshold. The initial threshold is determined as the average of the 5 first peaks. As the real heart rate of people is in the range of 40 to 220 beats per minutes (bpm), the 5 first peaks should occur in maximum 7.5 seconds or 2700 samples with the sample rate of 360 samples per second (Sps). Hence, at the beginning, we determine 5 maximum samples among 2700 samples. The counter variable The adaptive threshold is the average value of those 5 maximum samples. After that period, the adaptive threshold is updated as the average value of the 5 last detected peaks.

In addition, we only consider the next peak 127 samples (i.e. 0.35s) after the currently detected peaks as the next heart beat cannot occur during the current QRS complex. In the algorithm, we use a counter (variable Gap) to measure the period.

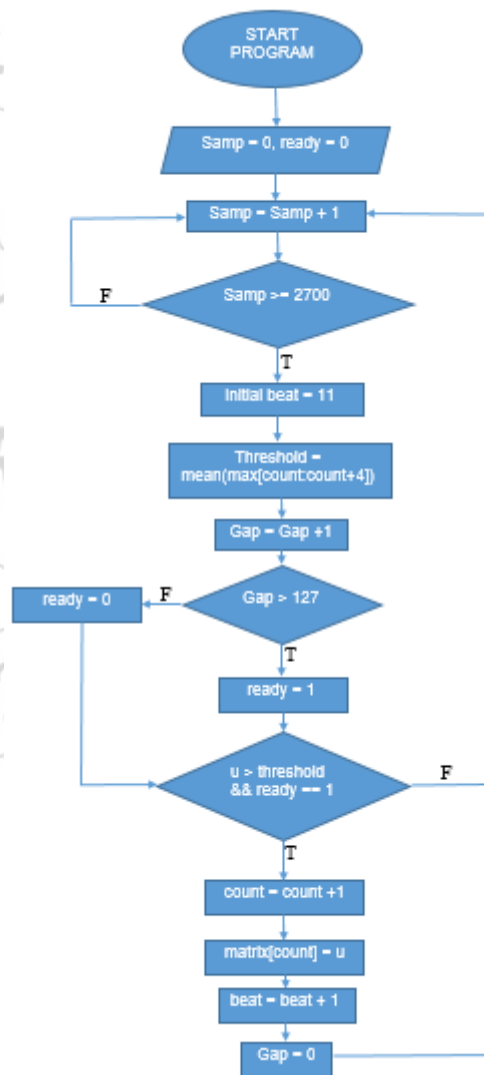


Figure 2: Heart beat detection algorithm

3. Hardware Architecture

The SoC used as ECG sensor node is shown in Figure 3. The SoC consists of three main components: (i) Microcontroller Unit (MCU); (ii) Analog front-end; (iii)

Power manager. The power manager takes energy from outside sources such as solar cells, RF or thermal energy harvesters and provides power for other components. The analog front-end amplified and sampled biological signals such as ECG, SpO₂, temperature. Last but most important, the MCU analyses the biological signals to provide us with useful information such as heart beats... The MCU consists of an ultra-low power processor, memory (such as ROM, RAM), programming/digital interface (such as JTAG, SPI, UART) and computational accelerators (such as bio-signal DSP, FIR, Heart rate detector, MAC). Computational accelerators release the central processor from computational tasks such that the processor can be in idle state most of the time, hence, consumes less energy. In this paper, we focus on designing the heart beat and QRS detection accelerator for the above mentioned SoC.

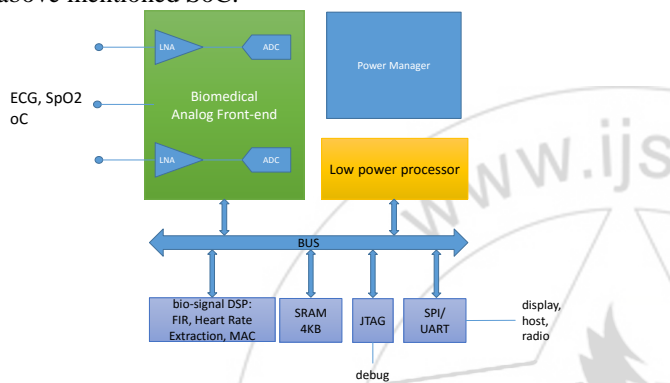


Figure 3: ECG SoC components

We design the accelerator using model-based methodology in Matlab/Simulink environment. The algorithm is implemented using sub-blocks provided by the HDL coder tool package. Then, HDL source codes are generated automatically by the tool. The Simulink model of the algorithm is described in detail in the following.

First, the MaMeMi filter being shown in Figure 5 is constructed from MaxCalculation, MinCalculation which are shown in Figure 5.

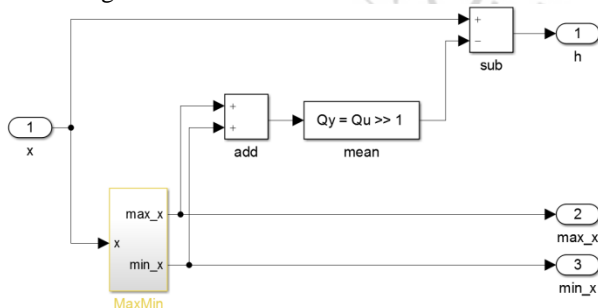


Figure 4: Hardware architecture of MaMeMi filter

In Figure 5, the register *initial_cnt* is used to initialize register *max_reg* which stores the *max** value of *x(t)*. At the reset, *initial_cnt* is 0 and *max_reg* is initialized by *x(0)*. After reset, *initial_cnt* is always 1 and *max_reg* is selected from two value *x(t)-delta* and *x(t)+delta*sigma* depending on the comparison between *x(t)* and *max**. The *min** of *x(t)* is calculated in the similar way.

Next, the high frequency pseudo noise is subtracted from the

MaMeMi output as defined in Eq. 5. Note that, the high frequency noise is the maximum-minimum range as defined in Eq. 4.

Afterwards, we will shape QRS complexes to triangles so that the beat detector can handle effectively as shown in Figure 7.

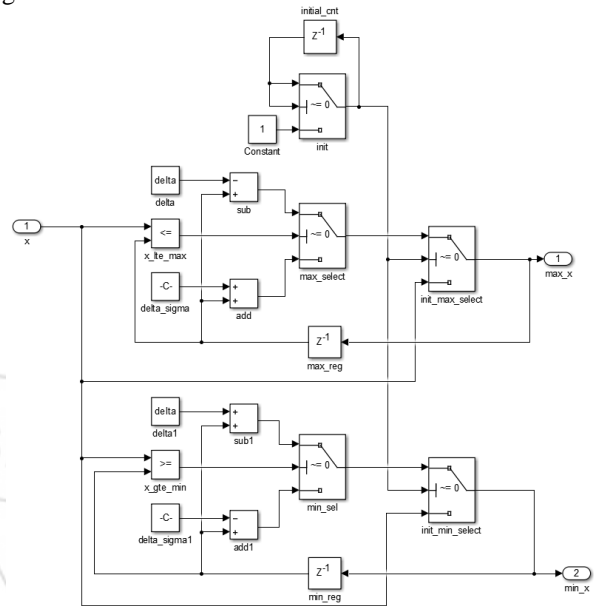


Figure 5: Hardware architecture of *max, *min****

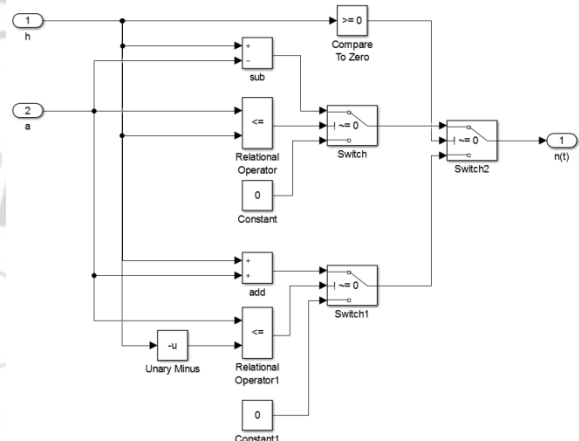


Figure 6: Noise subtraction

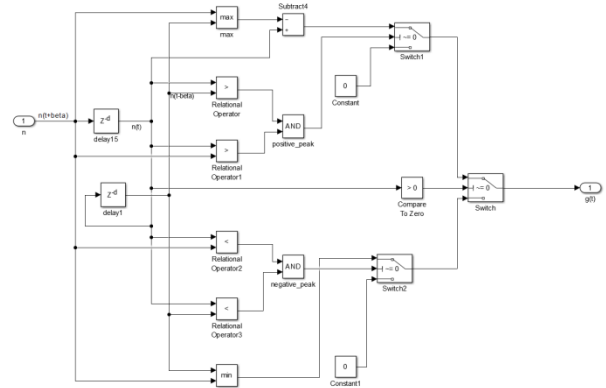


Figure 7: Triangular detector

Finally, the signal is compared with the adaptive threshold to detect the peak using the heart beat detector. The adaptive threshold algorithm is implemented in Matlab programming

language.

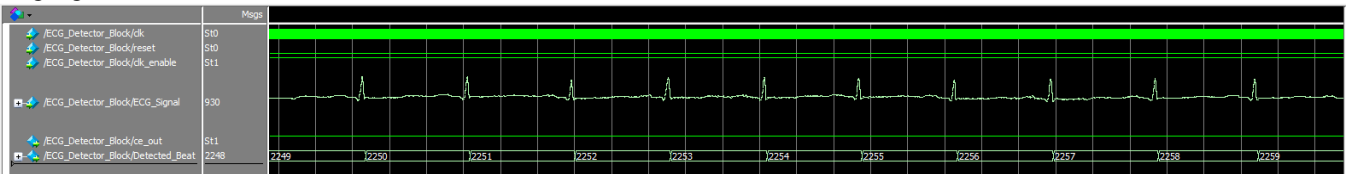


Figure 8: HDL Simulation Waveform

4. Experimental Results

We use Matlab/Simulink to design and validate the hardware design. First, we simulate the proposed architecture with the MIT/BIH arrhythmia database [**Error! Reference source not found.**] to evaluate the architecture accuracy. We count the number of detected beats by the proposed architecture and compute the detection error rate (DER). The proposed architecture achieves a detection rate of 98.88% with the DER is 1.117%.

After having good accuracy performance architecture, the Simulink architecture is automatically converted into HDL code using HDL advisor tool. The HDL code is then validated using the HDL simulator Modelsim. Figure 8 illustrates the correct behavior of the HDL code by a simulation waveform. As shown in the figure, the output *Detected Beat* increases by one when a beat occurs at the input *ECG_Signal*.

Finally, HDL code is synthesized into ASIC 45nm technology. Table 1 presents high level resource usage of the proposed architecture. The architecture occupies an area of 0.23mm² and consumes 1.26mW.

Table 1: High level resource usage

Multipliers	2
Adders/Subtractors	35
Registers	48
RAMs	0
Multiplexers	30

5. Conclusion

We have proposed a new simple, hardware-efficient architecture to detect QRS complex from ECG. The proposed architecture could archive the performance accuracy of 98.88% occupies only an area of 0.23mm² in ASIC 45nm technology and consumes 1.26mW at the clock speed of 100MHz. The proposed architecture is therefore very suitable for the ultra-low power SoC being used in ECG nodes.

6. Acknowledgements

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