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A Brief Overview of RFID Tag Design in FPGA

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Abstract: ***Radio Frequency Identification (RFID) now-a-days, widely using technology in the field of auto-identification of objects. The system consists of two basic blocks- tag and a reader. The tag is attached to the object to be identified and it transmits the identification number and other information to the reader. The reader after receiving the identification number or any other information processed it with the server. The major task performed in RFID system is done by the tag because it is attached to the distant object and also working in harsh environment. Thus the design of the RFID tag is the key issue of the overall system. Efficient performance and power optimization of the tag is required because tag is placed at a non contact distance from the reader so regular maintenance of tag is not possible. Many design of the tag have been proposed over many years which concerns performance, power optimization and security issues. In this paper a brief overview of the RFID tag design is discussed along with the comparative study of different design of the tag.***

Keywords: RFID, FPGA, EPC, VHDL

1. Introduction

RFID tag are basically of two types- active and passive. Active tags are having their own power source which provides power to the controller and also provides power for analog part of the tag for modulation of the tag. Passive tags are those which are not having their own power source thus along with receiving query from a reader they also receive energy and use this energy for responding a particular query. Passive tags are cheaper than active tags but there are some disadvantages of the passive tag-one is that the range of the passive tag is significantly lower as compared to the active tag and there is limited energy budget for passive tags thus the quality of the response is low. However, passive tags require less maintenance than active tags.[1]

Basically, the design of the RFID tag consists of two parts- analog front end and digital back end. The analog front end is responsible for the modulation and demodulation of the and the digital back end is responsible for the data processing such as instruction decoding and storage usually with the ROM.[4]. Many designs for the RFID tag has been undertaken in order to optimize the performance and cost factor of the tags and readers involved in RFID systems. FPGAs are considered as much efficient device for implementing RFID systems.[8]

2. Literature Review

In a paper presented by **Alex K. Jones, Raymond R. Hoare, Swapna R. Dontharaju, Shenchih Tung Ralph Sprang, Josh Fazekas, James T. Cain, and Marlin H. Mickle** in 2006 an ultra low power active RFID tag along with its automated design flow have been described. In this design the tag consists of a controller which can be easily work with different standards and custom proprietary commands. This tag design combined the properties of both the active and passive tags, that is it have the capability of active tag along with different power saving components by which the tag operated on a single battery throughout its lifetime. For reducing the power consumption a technique have been proposed which includes a burst switch. This switch makes the tag to remain asleep with its controller and transceiver either in hibernate mode or completely off. Also a smart buffer is also introduced which keeps the tag in a standby mode until it is needed. Several RFID tag system are considered for developing this design methodology. In all these designs various platform are provided for designing a tag controller. In first class design, the controller is designed by an embedded microprocessor core. In the second class design the embedded microprocessor is replaced by custom hardware controller. This controller is generated by the RFID compiler in synthesizable VHDL. In both technique two power saving components – burst switch and smart buffer is integrated with an existing transceiver. The smart buffer was implemented in FPGA. StrongARM, ESIC and Xscale are the three low-power embedded microprocessor which prototype the design Also an Actel Fusion, Xilinx Coolrunner II and direct ASIC implementation are the three hardware controller which are considered. [1]

A paper by **Jianping Wang Huiyun Li and Fengqi Yu in 2007** presented the design of RDIF tag based on a new structure as well as in this design, they focuses on the security issue and a new technique was proposed based on hash-lock structure. This makes the tag more secure than the non-security based tags. The security technique is based on a hash lock structure in which the tag sends hashed identification number to the reader, This function added the security to the tag, thus if the data sends by the tag is intercepted, the man-in-the-middle does not retrieve that information. The design is implemented in an Altera FPGA. In a new proposed system design the information which is stored in the RFID tag is reduced. In order to avoid the unethical tracking the tag baseband only consist of fixed unique serial number. The baseband of the tag is designed based on the new structure and the EPC (Electronic Product Code) Gen2 protocol. The design achieves high security level also its takes less logic gates by which 20% hardware reduction in the design is achieved. [2]

Su-Bong Ryu, Jin-Oh Jeon, and Min-Sup Kang in 2007 presents the design of Digital Codec for the passive RFID tag. The design is based on a mutual authentication protocol. This protocol is based on a three-way challenge response scheme for authentication between an RFID tags and the back end server. The design also modifies the ISO/IEC 18000-3 standard. This standard handles the communication between the RFID tags and a reader device, but security is not concerned with the above standard also there is no mechanism for authentication between the tag and the reader. Thus in the proposed design the ISO/IEC 18000-3 standard is modified and a hash algorithm known as Secure Hash Algorithm is used for authentication between the reader and the tag. The proposed design of the digital codec was explained using Verilog HDL at behavioral level and was synthesized for a Xilinx VertixII XC2V8000 FPGA device. The software tool used in the design is ISE 6.x and the timing verification of the system is performed in Modelsim. The design operates at a clock frequency of 75 MHz on the above mentioned FPGA device. [3]

In a paper presented by **Yujing Feng, Wei Zhang, Xiaohui Xing** the design of the baseband processing module for a 915 MHz Ultra High Frequency RFID tag is described along with a memory block. The design also considers the ISO/IEC 18000-6 Type B protocol and also supports some mandatory instruction. For working under tough clock conditions a novel clock generation block is also considered in the design. The mandatory instruction executed was GROUP_ SELECT_NE, READ and WRITE. The protocol ISO/IEC 18000-6 Type B is based on the reader talks first. The data transmission between forward link is achieved by the ASK modulation and the data rate is 10kbps or 40kbps, and the coding technique used in the design is Manchester coding technique. The module was developed in Verilog HDL. While designing the module in Verilog HDL hardware cost and area optimization was also considered. [4]

In a paper in 2009 **Jiaxin Wang and Dongkai Yang** presented a platform for a multi-protocol RDIF tag. Simulation which can be able to simulate multi UHF tag signals is simultaneously. There are many benefits and advantages o the above proposed design such as-

- **Supporting Multi Protocol**

EPCglobal™ Class-1 Generation-2 and ISO/IEC 18000-6B are the most famous standard in UHF band and simulation platform can be automatically or manually switch between these two protocols.

- **Multiple tag's simulation simultaneously**

In the supply chain activities there are many tags available in the readers reorganization range. The multiple signals are combined in one synthesis unit and then converted into analog signal by 16 bit DAC.

- **Collecting Data for future analysis**

The data received from the multiple tags to the reader is collected in a computer system and can be analyzed for improving the RFID system performance.

This simulation platform is based on a hardware which consists of a Texas Instruments TMS320C6173 digital signal processor and Altera Stratix II EP2S60 FPGA. By the simulation platform for the tag, the system performance could be verified. The platform shows a very good performance and also allows some basic configurations. This platform will be able to simulate multiple tags signal at the same time. Two protocols are supported by simulation platform- EPCglobal™ Class-1 Generation-2 and ISO/IEC 18000-6B. These protocols prove very easy in testing and verifying the UHF RFID readers. Anti-collision algorithm can also be improved in this design. The design provides flexibility in adjusting some parameters and in handling the future trends in supply chain. [5]

In a paper presented by **Erich Wenger, Thomas Baier, and Johannes Feichtner** a very flexible design approach is proposed for designing a RFID tag. In this approach a clone of ATmega128 processor is presented called as JAAVR (Just another AVR) and this JAAVR is used to build an RFID tag which can communicates through the ISO14443A standard. This proposed design will be able to process AES (Advance Encryption Standard), ECC(Elliptic Curve Cryptography) and hash functions. An JAAVR enabled RFID algorithm was build using 8.2KGE, which was verified as ASIC and FPGA, further the designed was extended with AES(+5.4KGE), hash function(+5.8KGE) and ECC(+9.7KEG). After that JAAVR performed over the air interface using RFID protocol various security. [6]

In a paper **Omar Abdelmalek, David Hely and Vincent Beroule in 2013** proposes a design methodology in order to develop a tag architecture which mainly focuses on security and authentication in which all RFID system parameters will be taken into account. In this paper the author highlights that RFID tags are mainly used in critical applications such as aeronautics and railways where they have to work in harsh environment. They provides security in applications such as identification, authentication etc. In such serious applications the malfunction of RFID chips may have serious consequences. Thus the robustness of the RFID tag must be increased in order to provide security for critical applications. The main purpose of this proposed work is to increase UHF tags robustness. For this, a validation methodology is proposed by the author with the platform for RFID IC. The new digital architecture of RFID is immune to hardware attacks and natural defects. This work specifically focuses on EPC Class 1 GEN2 Protocol which is the standard for UHF RFID long range identification at 860 -960 MHz The implementation of digital part of RFID tag baseband was designed by the VHDL code and software tool used for simulation is Xilinx tools. This simulation provides expected results. Functional verification can be performed by implementing the digital core in the FPGA. [7]

3. Conclusion

The design of the baseband of RFID tag implemented in FPGA provides flexibility to the design. Different design strategy will be developed to support different standards of UHF RFID tag and can be implemented easily in FPGA.

Various protocol was developed and security issue was also be added with the protocol. Various cryptographic techniques will be developed which provides security to the communication between the tag and the reader and avoid the possibility of eavesdropping and clandestine tracking. Thus design of the tag typical RFID system in FPGA improves various parameters of the overall system like performance, power optimization and security.

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