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Design of the Digital Baseband Part of an Active RFID tag in FPGA

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Abstract: ***RFID refers to Radio Frequency Identification which includes the use of a non-contact wireless system. The system uses the radio frequency electromagnetic waves for transferring the data from the tag which is attached to a particular object to be identified. The main purpose of the system is tracking and automatic identification of a particular object. Since the RFID systems are mainly non contact wireless systems in which the tag is attached to a distant object and have forced to work into harsh environment. Thus the optimization of performance and cost for the tags and readers of the RFID systems is the basic requirement mainly for the tag because in some applications the tag is placed in such places where the possibility of replacement of battery of the tag is almost negligible. The design of the tag must be power and performance oriented for long life of an RFID systems. FPGAs are considered as the most capable devices for implementing RFID systems. This paper presents the design of the digital baseband part of an active RFID tag in FPGA.***

Keywords: RFID, FPGA, EPC, VHDL

1. Introduction

Radio frequency identification (RFID) systems are progressing rapidly with their applications such as location sensing system, supply chain road tolling, building access control, aviation security etc.[1-2]. RFID tags do not need contact or precise aim with the target. The whole identification process can be finished without manual intervention. RFID tags can easily identify high-speed objects, be immune to oil and dirt operates in various environments, accommodate a large amount of data, and have a good capability of self-protection [3-4].

An RFID system composed of the tags and readers. The readers send instruction to the tag via an air interface, and the tag responds to the reader by sending a message back to the reader or by changing its current state.[5]

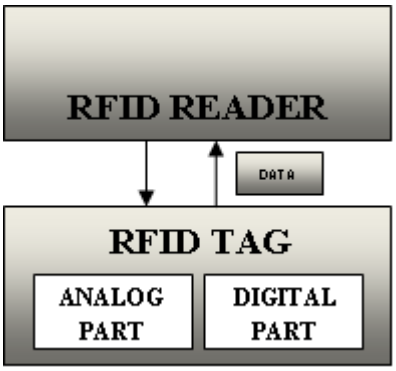

Figure 1: A simplified RFID system.

The tag consists of an analog part and a digital part. The analog part is responsible for providing power to the whole, modulating, demodulating, backscattering data to the reader and performs clock generation activities for the digital part. The digital part is responsible for data processing like instruction decoding and storage with a ROM. The communication between the tag and reader is established by the protocol which also take care of that data is transmitted without errors.[6-7]. Figure 1 shows the simplified RFID systems

In this paper the designing of the tag is done to support multi-protocol. A typical RFID tag respond one tag at a time, in this proposed design tag is developed in such a way that a reader will be able to respond multiple tags at the same time. This will reduce the cost of overall system and also enhanced the application of RFID systems in supply chain management.

The remainder sections of the paper are organized as follows: Section 2 describes the basic architecture of the tag design. Modules used in the design of the digital part of RFID tag is are briefly discussed in section 3. Results are related in section 4. Section 5 discusses conclusion and future direction.

2. Architecture

The blocks of the RFID tag is connected in a very efficient manner which enhanced the performance of the RFID system. For transmitting the information from the object Serial Communication Interface protocol is used which is developed by Motorola. The SPI protocol consists of SPI Master and SPI slave modules for establishing communication. The output of the digital part is captured through pulse width modulator and it further feed to analog part for modulation and demodulation purpose. Thus for interfacing the digital output to the analog input Pulse Width Modulator is a very efficient option. As the key concept is design is multi tag support the user logic must be written accordingly and for this design module the concept of state machine is used. This module also defines different states during the time of communication of the tag with the reader. Figure 2 shows the proposed architecture of the digital part of the RFID tag baseband.

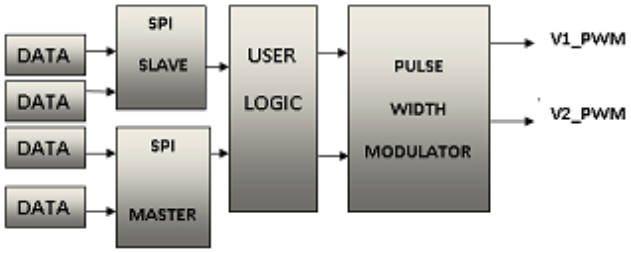

Figure 2: RFID- tag baseband architecture

3. Modules in the design of digital part of RFID tag baseband

A. SPI Master

A Serial Peripheral Interface is a protocol for serial transmission of data between Master and Slave. The main advantage of this protocol is that it is a full-duplex data link protocol. It has four basic pins. The transaction of data initiates by the master pulling Slave-Select (SS) pin low. There is a serial clock (SCLK) pin available for providing a synchronous clock source. There are two pins MOSI (Master out Slave In) for transmitting and MISO (Master In Slave Out) for receiving data.

B. SPI Slave

As discussed in the previous section, SPI Slave and SPI Master both are serially transmitting data to each other according to the user logic. The Slave transmits the data through MISO pin and receives the data through MOSI pin.

C. User Logic

The user logic module is the basic building block of the overall design of the RFID tag. This module describes the set of rules by which all the modules are communicated in such a way that the basic concept of the design must be fulfilled. This user logic will be designed by using the concept of state machine.

D. Finite State Machine

Finite State Machine is basically the sequential logic systems. A finite State Machine consists of some input, some outputs and a set of states and also some set of rules which defines transition from one state to other state.

E. Modulator

The final output of the baseband RFID tag is taken from this module. This digital block output is further feed as an input to the analog part of the tag for modulation and transmission to the reader. Thus for interfacing the digital output to analog part, pulse width modulator is a very potential and efficient module. Pulse Width Modulation is a very efficient technique by which analog circuits can be controlled by the PWMs digital output. By the use of the high resolution counters, duty cycle of square wave is modulated for encoding a particular analog signal level.

4. Results and Discussion

In the final implementation all the modules are put together to get the final output. For designing the proposed design in FPGA, the individual codes of all the modules is written in VHDL, then assembling of the modules is performed in the software tool Xilinx 9.1i. After assembling all the modules the RTL view of the final designed tag is simulated. The simulation is performed in Xilinx ISE simulator. There are 8 input pin and four output pins in a final design of the tag. Four input pins are required for SPI connection and two input pin are required for detection of oscillation. There are two output pins for SPI connection and two output pins for Pulse Width Modulator. Figure 1 shows the RTL view of the final design. All the blocks proposed in the architecture successfully connected in the final design of the tag.

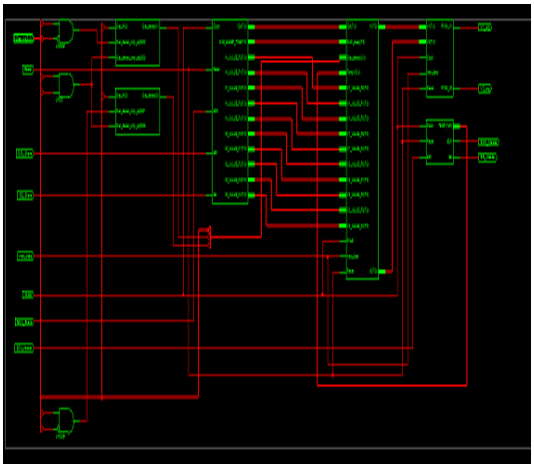

Figure 3: RTL view of the digital block of the tag.

The above block will be simulated in Xilinx ISE simulator. It is performed by generating a test vectors for different input values. The test vector will be generating by adding a test bench and then applying different possible combinations of the input. In the design Finite State Machine is the key block of the tag. There are five different states in the design of the tag. State machine controls all the other blocks of the tag as well as transition of the tag from one state to another is also decided by the state machine. The digital data is feed to the analog part of the tag for modulation and demodulation, Pulse Width modulator provides excellent interfacing with the analog part of the tag. The simulation output waveform of the input is shown in figure 4

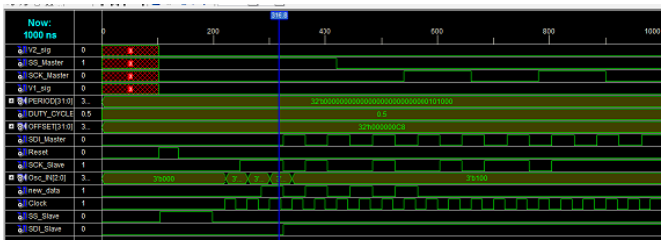

Figure 4: Simulation output waveform of digital block of RFID tag

5. Conclusion

In this paper, digital baseband of the active RFID tag with multi-tag support capability by the reader is designed. The tag supports the UHF band specified for the RFID tag.The SPI module is used for transferring data into the tag. This module will be on only when there is some data transfer takes

place thus the reducing the power consumption of the tag. As the active RFID tag has battery attached with it, the decrease in power consumption will increase the battery life as well as performance of the tag.

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