International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2015): 6.391

Design Approach towards the High Speed Circular Convolution by using UT Technique and High Speed Parallel Adder

Jamvant Omkar[1], Gurpreet Singh[2]

[1]M.Tech Scholar (VLSI), Trinity Institute of Technology and Research

[2]Professor (ECE Department), Trinity Institute of Technology and Research

Abstract: ***Now a day's digital devices are going to be a high compact and high portable with high speed designing technique. Digital signal processing and image signal processing is the vast area for researchers and convolution is the best technique for these techniques. In this paper we are designing a high speed convolution technique with low area and high speed. Convolution of the two sequences is the just like as multiplication. Here multiplier is the core element for designing the convolution, like wise adder is the main element+ or device for structuring the multiplier. There are three types of the convolution, Circular, linear and graphical. In this paper we are proposing circular convolution technique by using the Vedic mathematics fast calculation technique. Vedic mathematics is the Ancient Indian Fast calculation method. Modified parallel adder will be used for adding the high bit information. All the analysis and simulation will be done by Xilinx 14.2i software with Spartan 3 Series.***

Keywords: Circular Convolution, Linear Convolution, Parallel Adder, Vedic Multiplier (VM), UrdhwaTriyakbhayam Sutra (UT)

1. Object

The demands of the digital devices are increasing drastically. To full fill the facilities of the users we need some properties like low area, high mobility, high speed and low propagation delay. Generally convolution is used in digital signal processing. The object of this paper is to design the high speed convolution especially circular convolution.

2. Introduction

High convolution is the core element for digital processor or image processor. With the advent of new era of the digital devices speed of the processor must be high. Processor's speed can be enhanced by the aid of high speed multiplication and addition of the binary bits. With the latest advanced of VLSI technology we always keep in mind to increase the speed and reduce the area as possible as. Convolution and de-convolution techniques play an important role in digital signal processing and image processing. Convolution is a mathematical way of constructing two signals to form a third signal. on the other hand convolution is the process to the calculate the output signal for given input signal by using impulse response signal. Convolution is basically used in digital filter and correlation applications. Convolution can be segregated as linear, circular convolution and graphical convolution. Graphical method is the best way to represent the convolve of two signals but it is the tedious method,sogenerallyweuselinearandcirculartechnique in digital signal processing. Analysis of convolution depends on multiplier and adder devices. So in this paper we are using Vedic multiplier [1] which is based onUrdhvaTriyagbhayanm Sutra and Parallel high speed adder instead of traditional devices. Multiplication can be done by shifting and adding method but it gives high propagation delay. Another method is Wallace tree algorithm but it is not better than Vedic mathematics calculation.

$$y(n) = f(n) * g(n)$$

In above equation f(n) and g(n) are finite length sequence.

$$y(n) = \sum_{n=-\infty}^{+\infty} [f(k) * g(n-k)]$$

Linear Convolution can be calculated by using above equations. But this is lengthy process. This can be solved byseveral methods so cross multiplication is best method one of them. In the same manner circular convolution can be calculated.

3. Cross and Vertically Multiplication

Vedic mathematic is the group of 16 sutras which was proposed by Jagadguru Swami BharathikrishnaTrithaji of GovardhanPeeth, PuriJaganath (1884-1960). UdhvaTriyagbhayam sutra is essential technique for fast multiplication which is based on vertically and cross connections. This method is an essential technique for low power VLSI design and Digital signal processing.UrdhavTriyagbhayam is a novel concept through which throughput is obtained parallel and in short way. Generation of partial products and their summation is obtained using this algorithm which is explained in figure [1]. The main feature of this method that differs from other conventional process is that it reduces the need of resources from process to operate at high frequencies requires. The core factor of Vedic multiplier based on UrdhavaTriyagbhayam method [2] is that as the number of bits increases, area and gate delay increases at a faded rate as compared to other multipliers. Figure [1] gives the idea about the binary cross multiplication by using UdhvaTriyagbhayam Vedic multiplication technique.

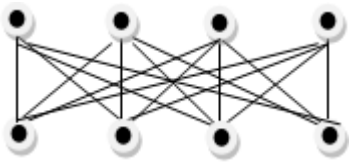

Figure 1: A Vedic cross multiplication technique to multiply 4 bit information

Here (A_3, A2, A1, A0) upper solid point and (B_3, B2, B1, B0) bottom solid points bits are multiplied together and produce 8 bit output sequence. Firstly A_0 is vertically multiplied with B_0 that would be the first product bit. It can be designed by using the simple AND gate. For the second product bit A_1 is cross multiplied with B_0 and A_0 is cross multiplied with B_1 then both partial product will added by using the half adder device. Next product bit can be computed by using vertically and cross multiplication, A_2 is diagonally partial multiplied with B_0, A_0 is cross multiplied with B_2 and A_1 is vertically multiplied with B_1, now these bits can be added by using half adder and full adder.In the same manner other remaining bits can be found. UdhvaTriyagbhayam sutra [9] is one of the most techniques for the multiplication technique from other technique. By the aid of this technique number of computing steps can be reduced. Number of gates and elements are dependent on calculation of steps. Further this method can be enhanced for 8 bit, 16 bit and 32 bit parallel adder. So, Vedic mathematic provides the less complexity then to other calculation techniques.

4. Modified Method for the Circular Convolution

Convolution of the two sequences is the just like as multiplication of the binary bit information. There are three types of the convolution, linear, graphical [3] and circular convolution. In this paper mainly focused on circular convolution.

Circular Convolution

Circular convolution is the most frequently used in filtering the noise and blurred signal in digital signal processing and image signal processing. Circular convolution has many applications and is usually applicable to electrical engineering students in a digital signal processing. The Vedic mathematics multiplication is a novel method for computing the circular convolution [4]. Circular convolution can be obtained by using the shifting and folding technique but it gives complicated solution. So in paper we are using Vedic multiplication and parallel addition to compute the circular convolution sequence. Let us assume that f(n) and g(n) are finite length sequence then output of circular convolution y(n) is

$$y(n) = f(n) * g(n)$$

$$y(n) = \sum_{n=0}^{N-1} [f(k)g(n-k)(ModN)]$$

Where, N is the length of the sequences. for instance one finite length sequence is (A_3,A_2,A_1,A_0) and another sequence is (B_3,B_2,B_1,B_0) then output sequence for circular convolution is (Y_3,Y_2,Y_1,Y_0).

$$Y_0 = A_0 * B_0 + A_3 * B_1 + A_2 * B_2 + A_1 * B_3$$
$$Y_1 = A_1 * B_0 + A_0 * B_1 + A_3 * B_2 + A_2 * B_3$$
$$Y_2 = A_2 * B_0 + A_1 * B_1 + A_0 * B_2 + A_3 * B_3$$
$$Y_3 = A_3 * B_0 + A_2 * B_1 + A_1 * B_2 + A_0 * B_3$$

In circular convolution no carry out will be propagated to other equations.

5. Modified Steps to Design High Speed Convolution

Regarding the steps of the high speed convolution designing there are two steps. First is to construct a high speed parallel adder like Kogge-Stone adder[3]. Second is to design low area multiplier which can multiplied with low propagation delay. Logic diagram of the adder will be designed by stepping method. In this method 4 bit multiplier is designed by 2 bit multipliers and adders. Likewise 8bit multiplier [5] is constructed by using 4 bit multipliers and adders.

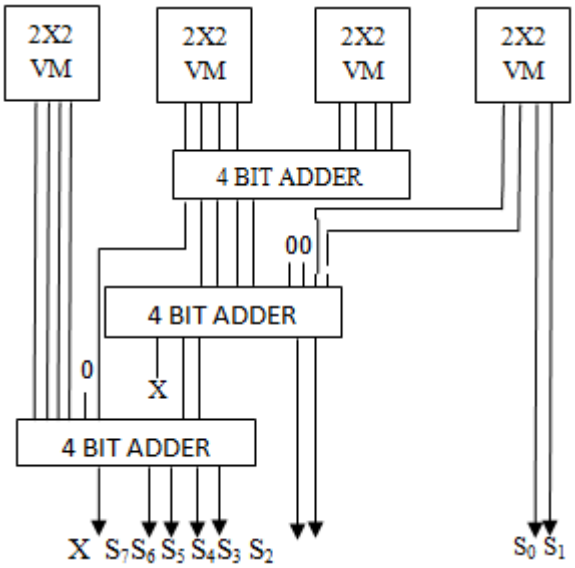

Figure 2: A 4 bit High Speed 4 bit Vedic Multiplier by using 2 bit Adder

Figure [2] shows the 4 bit multiplier by using 2 bit Vedic multipliers. Output of the 4 bit multiplier must be in 8 bit. Here in this logic diagram X denotes the not connected with any device. And zero value indicated the extra value which is connected with the adder device. Adder is the digital device which can add 4 bit or more than 4 bit information in parallel form. By the aid of parallel adder high speed multiplier circular convolution can be designed. Let us assume that we are having two sequence (4,3,2,1) and (3,2,1,1) then circular convolution of these sequence will be (15,9,22,17). Circular convolution is just like as multiplication of the two digits with shifting, but difference is that there is no carry forwarding system. To design Circular convolution 8bit [7] and 9bit adders are needed.

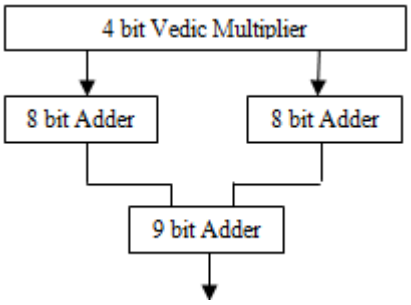

Figure 3: Modified 4 bit Circular convolution.

According to this logic diagram 4 bit multiplier gives the 8 bit output and these outputs will be added by 8 bit adder. Adder of the 8 bit information gives the 9bit output information. These 9bit can be added by 9 bit adder.

6. Software Tool

All the simulation and synthesisis done by 14.2i Spartan 3 series Xilinx tool. This is an advanced tool which provides less propagation delay than to 6.2i and 9.2i Xilinx tool. The most important advantage of this tool has less memory with high speed analysis any complex logical circuit.Simulation and synthesize of convolution logical circuit can be enhanced by Xilinx design suit 14.2i Spartan 3 series and device XC3S400-5fg320.

7. Comparison of Modified Circular With Conventional Convolution

Proposed enhanced speed circular convolution which is comprised with Vedic multiplier and Parallel adder can compare with conventional method which is computed by Vedic multiplier, full adder and half adder [8]. Proposed technique provides less path delay and less area. Input sequence of Conventional method is much more than to proposed method, however proposed method has less propagation delay.

Table 1: Comparison between Conventional circular and Modified High Speed circular Convolution

Parameter	Conventional Circular convolution	Modifiedcircular convolution
No of slices	358	315
No of IO Buffers	96	72
No of LUTs	623	560
Propagation Delay	21.963ns	16.505

Table [1] shows the comparison of the conventional and modified high speed convolution technique. The parameters are I/O sequence, slices, input output buffers, and look up table (LUTs) and propagation delay that is also called combinational path delay. Number of slices of the conventional method [9] is less than to modified convolution technique. Number of the input, outputs buffers is having same value for both. The main motive of this paper is to reduce the propagation delay. Propagation delay is an essential parameter to design the high speed convolution technique.

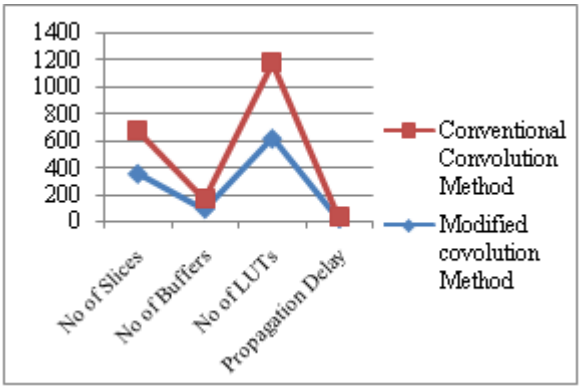

Figure 4: Graph between the Conventional and Modified Linear Convolution Technique

Above graph shows the parameter comparison between conventional and modified 4 bit linear high speed convolution technique. The no of slices and LUTs are more but propagation delay is less. Main object of the paper is to reduce the propagation delay. Propagation delay or combinational path delay is essential parameter than to other parameters.

8. Conclusion& Future Scope

Finally proposed circular convolution has less area and slices than to convectional technique.Regarding the propagation delay simple Vedic multiplication using linear convolution has 45% more than to convolution using the Vedic multiplication as well as Parallel adder. Designed high speed convolution technique can use for designing the filter to filter the blurred signal [10]. This can be used for image processing and digital signal processing technique. By using high speed multiplier ALU, GPU and CPU can be designed.

Refrences

[1] PushpalataVerma, 2012.Design of 4x4 bit Vedic Multiplier using EDA Tool, International Journal of Computer Applications, vol.48, no.20, 2012.
[2] Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, 2009.High speed energy efficient ALU Design using Vedic multiplication techniques, IEEE Int. Conf. on Advances in Computational Tools for Engineering Applications (ACTEA2009), pp. 600-603, July 15-17, 2009.
[3] Y. Choi, 2005.Parallel Prefix Adder Design, Proc. 17th IEEE Symposium on Computer Arithmetic, pp 90-98.
[4] Kogge P and Stone H, 1973.A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Relations, IEEE Transactions on Computers, Vol. C-22, No. 8, pp. 786-793.
[5] Madhu Thakur and Javed Ashraf, 2012.Design of Braun Multiplier with Kogge-Stone Adder and Its Implementation on FPGAInternational Journal of Scientific and Engineering Research, Vol. 3, No. 10, pp. 03-06, ISSN 2229-5518.
[6] SomayehBabazadeh and MajidHaghparast, 2012.Design of a Nanometric Fault Tolerant Reversible Multiplier

Circuit, Journal of Basic and Applied Scientific Research.

[7] PakkiraiahChakali and Madhu Kumar Patnala , 2013.Design of High Speed Kogge-Stone Based Carry Select Adder, International Journal of Emerging Science and Engineering (IJESE), Vol. 1, No. 4, ISSN: 2319-6378.

[8] Lomate, Rashmi k and p.c. Bhaskar "High Speed Convolution and deconvolution using Urdhva Triyagbhyam" VLSI (ISVLSI), 2011 IEEE Computer society annual symposium on IEEE, 2011.

[9] Itwadiya, Akhalesh K, et al "Design a DSP operations using Vedic mathematics" Communications and Signal Processing (ICCSP), 2013 International Conference on IEEE,2013.

[10] Rashmi Lomte and Bhaskar P.C., "High Speed Convolution and Deconvolution using UrdhvaTriyagbhyam " ,2011 IEEE Computer Society Annual Symposium on VLSI ,p.323 ,July 2011.

[11] John W. Pierre, ―A Novel Method for Calculating the Convolution Sum of Two Finite Length Sequences‖, IEEE transaction on education,VOL.39, NO. 1, 1996.

[12] MadhuraTilak ―An Area Efficient, High Speed Novel VHDL Implementation of Linear Convolution of Two Finite Length Sequences Using Vedic Mathematics‖, IJITEE Volume-2, Issue-1, December 2012.

[13] Hsiao, Shen-Fu, Ming-Roun Jiang, and Jia-SienYeh, "Design of highspeed low-power 3-2 counter and 4-2 compressor for fast multipliers," IEEE Electronics Letters, vol. 34, no.4, pp. 341-343, Feb. 1998.

[14] Jagadguru Swami Sri BharatiKrisnaTirthaji Maharaja, "Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda," pp. 5-45, MotilalBanarasidas Publishers, Delhi, 2009.

[15] D. Radhakrishnan and A. P. Preethy, "Low power CMOS pass logic 4-2 compressor for high-speed multiplication," Circuits and Systems, Proc. 43rd IEEE Midwest Symp., vol. 3, pp. 1296-1298, 2000