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# Implementation of Low Power Adiabatic based Inverter for Dynamic Comparator

**Heena Parveen[1], Vishal Moyal[2]**

[1, 2]Department of Electronics & Telecommunication Engineering, SSTC, SSITM, Bhilai, India

**Abstract:** ***The requirement for portable battery operating devices is escalating nowadays, hence low power methodologies are being favoured for high speed applications. Symmetric circuits with regenerative feedback provide opportunity to spot new structures that may be mainly helpful. Regenerative feedback is generally used in Dynamic Comparators and hardly ever in non clocked comparators. In the process of designing high speed ADCs (Analog-to-Digital Converters), Dynamic Comparator is generally used and can be simply designed. Dynamic comparators have a wide use in high speed ADCs because of their fast speed, high input impedance, full-swing output and low power consumption. To further reduce the power consumption, a novel Dynamic Comparator has been proposed where the back-to-back inverter of a conventional dynamic comparator is being replaced by the DFAL (Diode Free Adiabatic Logic) inverter that utilizes the adiabatic logic principle. For the corroboration of performance, the design is simulated by the Cadence Virtuoso Spectre simulator in gdpk 90nm Technology.***

**Keywords:** Conventional Dynamic Comparator, CMOS inverter, Adiabatic Logic, DFAL inverter

## 1. Introduction

The comparator is considered to be an important analog circuit that is required as a main part in Analog-to-Digital Converters (ADCs). Comparator basically compares one input voltage signal against another voltage signal and a binary output signal is generated as per the comparison. Dynamic Comparators which fall under the category of regenerative comparators have a wide use in high speed Analog-to-Digital Converters [1] owing to their lesser power dissipation, high speed and no static power consumption. Despite having such benefits, Dynamic Comparators suffer from certain device mismatches [2] such as parasitic node capacitance, threshold voltage and current factor β which are the prime reason for causing random offset voltages in comparators by deteriorating their performance. Employing offset cancellation or calibration techniques [3-5] while implementing comparator is also an effective methodology to alleviate this issue. Moreover, the reduction in the offset voltage can be done by means of a preamplifier in the design of comparator, but at the cost of more power consumption and complexity.

It is also observed that in conventional CMOS circuits, the power consumption is proportional to the square of the supply voltage and load capacitance [6], thus the researchers are focussing on supply voltage scaling and reducing the circuit capacitance so that the power consumption can be reduced. For supply voltage scaling, the threshold voltage ($V_t$) of transistor should be proportionally scaled down, though reducing the threshold voltage ($V_t$) of transistor result in a proportional increase in sub-threshold leakage current. The circuit capacitance could be further minimized by a reduction in the device sizes, but this will affect the driving capability of the circuit.

Because of these constraints, in current era, adiabatic logic systems have been used with the intention of reducing the power consumption. Different adiabatic logic circuits have been proposed [7–14] based on the functioning of charge recovery principle. Adiabatic logic circuits [15] are considered as low power circuits which make use of reversible logic [16] for conservation of energy. Adiabatic logic is an attractive low power methodology which can be used as an alternative to standard CMOS circuits by providing means of reusing the energy that is stored in the load capacitor instead of following the usual means of discharging the load capacitance to the ground and wasting this energy.

## 2. CMOS Inverter

In the conventional CMOS circuits, the occurrence of power dissipation arises mainly during the device switching. During the voltage transition of the nodes, the power is dissipated while charging or discharging of the parasitic capacitances throughout the switching operation. A node capacitance $C_L$ is charged from 0 to $V_{dd}$, and an amount of energy = $V_{dd}$.Q ($=C_L V_{dd}^2$) is drawn from the supply. During the phase when the charge is going up, one half of the energy, i.e. ½ $C_L V_{dd}^2$ is dissipated as heat in conducting PMOS transistor, and the other half energy i.e. ½ $C_L V_{dd}^2$ is stored in load capacitances. During the phase when the charge is going down, the energy that has stored in output load capacitance is dissipated in nMOS transistor. This switching energy dissipation could be minimized by a reduction in the physical capacitance and supply voltage. But there exists a drawback when the supply voltage $V_{dd}$ reduces, i.e. increase in the sub-threshold leakage current. Reduction in the circuit capacitances can be done by reducing the device sizes, however this will affect the driving capability and speed of the circuit.

## 3. DFAL Inverters

The circuit diagram of a DFAL inverter is shown in figure 1. These circuits have an attractive feature that they are free of diodes i.e. there are no diodes in their charging/discharging

path. It consists of two split-level sinusoidal power clock supply $V_1$ and $V_2$ where one of the clocks will be in phase whereas the other one will be inverted. The voltage level of $V_1$ exceeds $V_2$ by $V_1/2$ which will minimize the voltage difference between the electrodes and this will result in the reduction of power dissipation. Charging and discharging of the load capacitance by the split-level power clock is relatively slower than other adiabatic power clocks. As the efficiency of adiabatic circuits depends on how slow the load capacitance charges/discharges, the power dissipation can be further minimized.

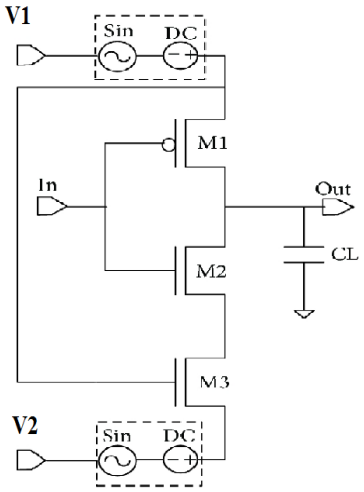


**Figure 1:** DFAL Inverter

The resemblance of the static CMOS logic can be seen in the schematic of DFAL; however the circuit operation is in adiabatic mode. In the pull down network, the nMOS transistor (i.e. Transistor $M_3$) which is adjacent to the transistor $M_2$ is being used as a replacement of the diode for discharging. Power clock ($V_1$) controls the turning ON and turning OFF of this transistor ($M_3$). In other adiabatic circuits, the main power dissipation which occurs at the diodes is because of the drop in threshold voltage (non adiabatic losses) at their discharging path while in DFAL circuits, it's because of the ON resistance (adiabatic losses) of the channel of transistor $M_3$. The power dissipation owing to the ON resistance (of transistor $M_3$) is considerably lower than the power that has been dissipated because of the drop in threshold voltage through the diodes. Moreover, this MOS transistor $M_3$ recycles charge from the output nodes and thus the further recovery of adiabatic losses can be done. But, still the power dissipation could not be removed totally and losses could not be fully recovered since the DFAL circuits are non reversible logic circuits. Therefore, the power dissipation is massively reduced in comparison to the adiabatic circuits (diode based) via the MOS transistor M3.

## 4. Dynamic Comparators

Dynamic Comparators are often described as Clocked comparators. Regenerative feedback is generally used in Dynamic Comparators and hardly ever in non clocked comparators. The conventional dynamic comparator which has a wide use in analog-to-digital converters is shown in figure2. Its operation is explained as follows: Dynamic Comparators have two operating modes: reset and evaluation phase. These operating modes operate as per the clock input that is provided to the circuit.

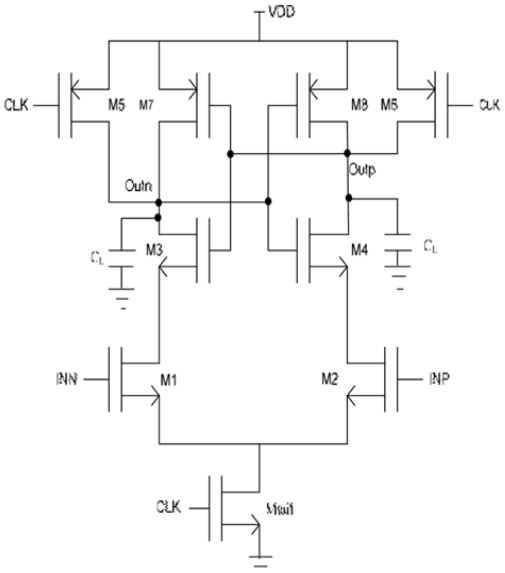


**Figure 2:** Conventional Dynamic Comparator

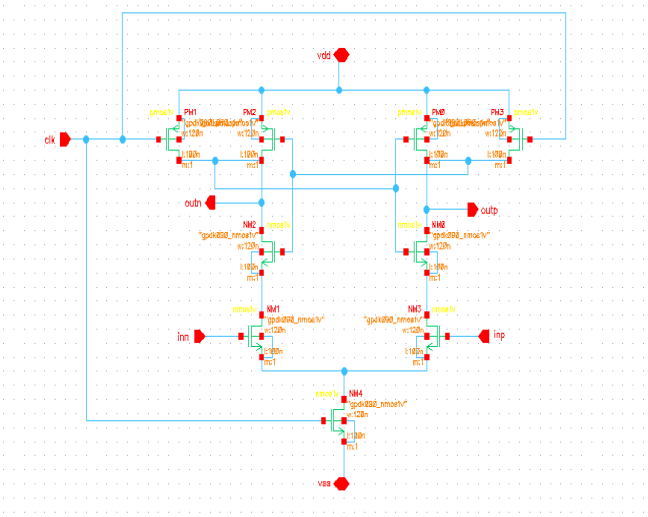

**Figure 3:** Schematic of Conventional Dynamic Comparator

When clock input is LOW in reset phase, transistor $M_{tail}$ will be in OFF state. The reset transistors ($M_5$ and $M_6$) will become ON and will pull both the output nodes (i.e. $Out_n$ and $Out_p$) to voltage $V_{dd}$ for initiating the starting condition. During the evaluation phase, when the clock input becomes HIGH, transistors $M_5$ and $M_6$ will become OFF and simultaneously $M_{tail}$ will be ON due to which $Out_n$ and $Out_p$ which were at $V_{dd}$ will start falling with different rates of discharging. The case when $V_{INP}$ is found to be greater than $V_{INN}$, here the voltage at $Out_p$ will discharge faster than that of $Out_n$. Since the voltage at the node $Out_p$ is discharged by the drain current of transistor $M_2$, the voltage will fall down to $V_{dd}-|V_{thp}|$ before the voltage at node $Out_n$ is discharged by the drain current of $M_1$, as a result of which transistor $M_7$ will be ON. Consequently, the back-to-back inverters will begin the latch generation and the voltage at node $Out_n$ will become $V_{dd}$ and the voltage at node $Out_p$ will fall down to the ground. The case when $V_{INN}$ is found to be greater than $V_{INP}$, the circuit will work in a vice versa manner.

## 5. Proposed Dynamic Comparators

Figure 4 describes the schematic diagram of the proposed dynamic comparator. The main objective of the proposed comparator is to reduce the power consumption of the conventional dynamic comparator by a certain level, by replacing its back-to-back inverter with a DFAL inverter that shows lower power consumption than the CMOS inverter.

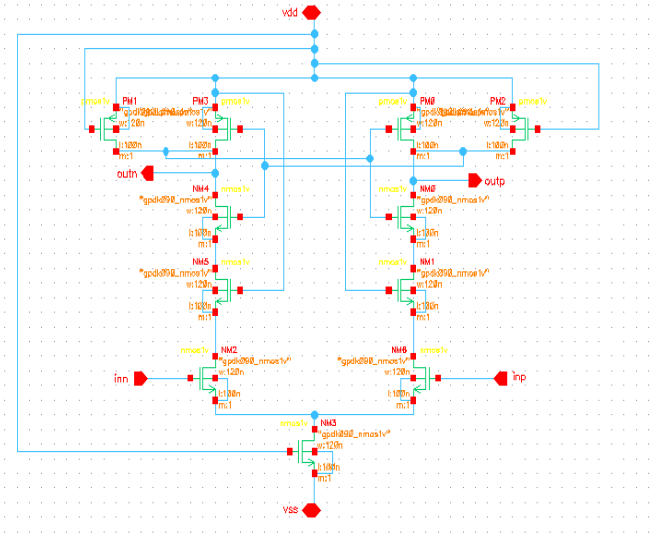


**Figure 4:** Schematic of Proposed Dynamic Comparator

## 6. Simulation and Results

The Proposed Dynamic Comparator and Conventional dynamic comparator are designed and simulated by the Cadence Virtuoso Spectre simulator in gdpk 90nm Technology at a supply voltage of 3V. The Proposed Comparator as designed uses low power when compared against Conventional Dynamic Comparator.

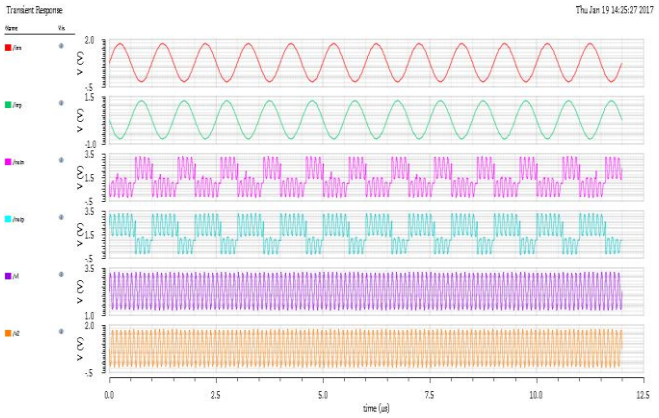

**Figure 5:** Simulation output waveform of Proposed Dynamic Comparator using DFAL Inverter

### 6.1 Comparison of Proposed Dynamic Comparator with Conventional Dynamic Comparator

The performance of conventional and proposed dynamic comparator based on CMOS and DFAL inverters respectively has been calculated by varying the input frequency and load capacitances with respect to power and are shown in Tables 1 and 2 respectively. For analyzing frequency, load capacitance has been set to 1 fF and for analyzing load; power clock frequency and input have been set to 10 MHz and 1 MHz, respectively.

**Table 1:** Comparison of power at 1fF in 10 clock cycles of charging or discharging

| Frequency | Power Dissipation (µW) | | Power Saving (%) |
|---|---|---|---|
| | Conventional Dynamic Comparator | Proposed Dynamic Comparator | |
| 1 MHz | 23.88 | 2.127 | 91.09 |
| 2.5 MHz | 24.84 | 3.164 | 87.26 |
| 5 MHz | 25.23 | 3.303 | 86.91 |
| 8 MHz | 24.31 | 4.202 | 82.71 |

**Table 2:** Comparison of power at 1MHz in 10 clock cycles of charging or discharging

| Load Capacitance | Power Dissipation (µW) | | Power Saving (%) |
|---|---|---|---|
| | Conventional Dynamic Comparator | Proposed Dynamic Comparator | |
| 1f F | 23.88 | 2.127 | 91.09 |
| 5f F | 23.89 | 3.502 | 85.34 |
| 10f F | 23.94 | 5.958 | 75.11 |
| 15f F | 23.99 | 6.438 | 73.16 |

## 7. Conclusion

The results of simulation and evaluation of performance comparison show that the consumption of power in the proposed dynamic comparator is lower than the conventional dynamic comparator and provides 91.09 % of power saving at 1 MHz. The Proposed Dynamic Comparator would be very effective in high speed ADCs and other VLSI applications.

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