A Comparative Study of Total Harmonic Distortion in Multi-Level Voltage Source Inverter

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Abstract: *Reduction the harmonic contents in the output voltage waveform of the Voltage Source Inverter (VSI) is of primary concern. Different control strategies were developed to reduce the harmonic contents of voltage waveform. In this context, pulse width modulation (PWM) control strategy is well known. Unfortunately, itsoutput controllability is limited since the modulation index and the chopping-to-supply frequency ratio, which are the only control parameters, have fixed values. In this paper, a multi-level voltage source inverter with improved harmonic elimination capability is presented. The output voltage waveform is developed through a multi-stage dc link. The performance and the total harmonic distortion of the proposed design are compared for different number of output voltage levels. Moreover, a comparison is also made with a sinusoidal-pulse-width-modulation (SPWM) inverter. Results show that the inverter presented, when compared to conventional multi-level counterparts and to that using SPWM technique, provides lower value of the THD factor. In addition, increasing the number of the voltage levels of the proposed inverter circuit reduces further the THD factor of the output voltage waveform.*

Keywords: Total Harmonic Distortion, Multi-Level Voltage Source Inverter

1. Introduction

The inverter is a power conversion circuit that operates from a dc voltage source or a dccurrent source and converts it into a symmetric ac voltage or current by which both magnitude and frequency can be controlled. Theinput dc supply of the inverter can be a battery system, a photovoltaic system or a dc source derived from an ac source [9,10]. According to the input supply used, inverters are classified as current-source inverters (CSI) and voltage-source inverters (VSI). The input supply of the CSI is a dc current source, while that of the VSI is a dc voltage source. The CSI circuit has direct control over the output (ac) current. The shape of the output current waveform of the ideal CSI is independent of the load connected at its output. CSIs are generally used for ac motor drive applications. Opposing to the CSI, the input supply of the VSI is a stiff dc voltage source [3].

In square wave inverters, maximum output voltage can be obtained. However, the output voltage waveformscontain all the odd harmonic components and hence, proper output filtration has to be used to reduce the harmonic contents and to improve the voltage waveform quality.

Several pulse-width modulation (PWM) techniques are used to decrease the harmonic contents of the inverter output voltage waveform and to generate an output voltage waveform that is close to the sine wave. In practice, sine-wave pulse-width modulation (SPWM) technique is the most popular technique used in controlling voltage source inverters.

Multilevel voltage source inverters offer high power capability, associated with lower output harmonics and lower commutation losses. As compared with the PWM inverters, although multilevel inverters require greater number of power devices, the size and thus the cost of the filters attached at the output of the multilevel inverters is lower than that for SPWM inverters.

In this paper, a multilevel voltage source inverter with improved harmonic elimination capability, as presented in [1, 2] is analyzed. The multi-level output voltage waveform of this inverter is developed through a multi-stage dc link. The output voltage waveform of this inverter is free from the most undesired existing harmonics. The performance of studied multilevel inverter, specially the total harmonic distortion, is studied for different number of stages of the dc link. Also as most of the practical today's voltage source inverter are implementing SPWM technique, the performance of the studied multilevel inverter is compared with its counterpart using an SPWM technique.

Section 2 reviews some of the related works, section 3 explores the power circuit configuration and principle of operation, section 4 demonstrates the main obtained results with a discussion and evaluation for those results, section 5 concludes the conducted work in this paper and section 6 demonstrates some of the work that can be performed in the future to enhance the current work.

2. Related Works

Many researches for improving the harmonic contents and decreasing the total harmonic distortion factor of the voltage source inverters have been previously done. [2] proposed a single-phase multi-level multi-stage dc link voltage source inverter with improved harmonic elimination capability. The multi-level output voltage waveform, of the proposed inverter, is developed through a multi-stage dc link [8]. A 3-stage dc link that provides 7-level of the output voltage waveform was used. The first five lower-order harmonics (i.e., 3rd , 5th, 7th, 9th, and 11th) were eliminated.

The controllability achieved by the programmed PWM schemes, mentioned by [4-7]are claimed to provide higher system controllability than that provided by the carrier-modulated PWM techniques. This is due to the fact that In case of carrier-modulated PWM, the controllability of the system is limited since the modulation index and the

chopping-to-supply frequency ratio, which are the only control parameters, have fixed values. According to Carrara et al, theoretical analysis of multi-level PWM technique, to eliminate certain harmonics from this waveform, is developed. In this reference the use of the multi-level output voltage waveform, to eliminate certain harmonics, is referred as "harmonic cancellation technique".

The work by [10] presents a five-level inverter that can be used for the drive of large induction motors. The switching elements used in the discussed inverter were the gate-turn-off thyristors (GTO). A multi-level voltage-source inverter with separate dc sources used for static VAR generation (static VAR compensator) is presented by [11,12] presents a High power factor ac/dc/ac converter with H-bridge cascade five-level PWM inverter. This converter includes an ac/dc converter for producing the dc voltage required to supply the inverter [5,6].

3. Power Circuit Configuration and Principle of Operation

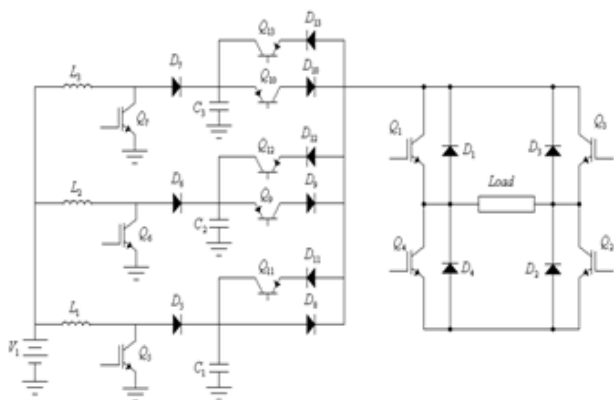The power circuit configuration of the multi-level VSI under study is shown in the figure below.

Figure 1: Power Circuit Configuration of the Multi-level VSI [3]

In this circuit, a VSI with 3-stage DC link is shown. This circuit can be expanded to include different number of DC links. The 3-stage multi level VSI shown in the above figure is capable to generate a 7-level output voltage waveform. In general, an m stage DC link is capable of generating a 2M+1 voltage levels in the output voltage waveform of the multilevel VSI. The switching pattern of the system elements ensure the required switching from one voltage level to another. As shown from figure 1, the system under consideration consists of the following building blocks:

- An H-bridge inverter, that consists of the four transistor switches $Q_1 - Q_2$ and the four anti-parallel diodes $D_1 - D_2$. The transistor switches are driven to ensure the required output frequency and to force the zero-voltage level of the output voltage waveform, where applicable.
- Three identical boost converters that generates the required voltage levels V_1, V_s and V_3 that satisfies the requirements of the output voltage waveform. Q_5, D_5, L_1 and C_1 are the elements of the first boost converter that generates the first voltage level V_1. Q_6, D_6, L_2 and C_2 are the elements of the second boost converter that generates

the second voltage level V_2 and Q_7, D_7, L_3 and C_3 are the elements of the third boost converter that generates the third voltage level V_3.

- A feedback circuitry, this circuitry is added to provide feedback paths during the periods over which the load voltage and current waveforms have different polarities. Such periods, and hence the conduction pattern of the switching devices of this controller, are load-dependent. Q_{11} and D_{11} are able to conduct over the period of the first voltage level $\pm V_1$, Q_{12} and D_{12} are able to conduct over the period of the second voltage level $\pm V_2$ and 3 and D_{13} are able to conduct over the period of the third voltage level $\pm V_3$.
- A controller, designed to feed the outputs of the boost converters V_1, V_2 and V_3 to the inverter circuit at the angles α_1, α_2 and α_3 respectively. D_3 feeds a voltage level of V_1 at α_1, Q_9 and D_9 feed a voltage level of V_2 at α_2 and Q_{10} and D_{10} feed a voltage level of V_3 at α_3. Zero-voltage levels are forced during freewheeling periods of inverter operation, during which Q_1 and D_3 or Q_3 and D_1 are conducting. A typical switching pattern of the elements is shown in the figure below.
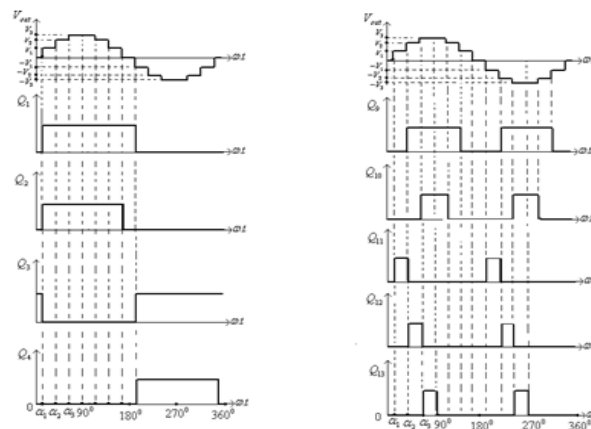

Figure 2: Typical Switching Pattern of a 3-stage Multi-level VSI [3]

The following table summarizes the inverter output voltage and the states of the transistor switches at the first quarter of the first half period of the output voltage waveform.

4. Simulation Results

As known, the operation of the SPWM inverter is based on comparing a triangular carrier signal with a sinusoidal modulating signal. The harmonic contents of the output voltage waveform of the SPWM inverter is a function of both the frequency of the triangular carrier signal (f_c) and the modulation index (m_a) As a result of this program, the figures below show the output voltage waveforms and the harmonic contents of these waveforms at different carrier frequencies and different values of the modulation index.

From these figures, the output voltage waveform of the SPWM inverter contains harmonics of several orders. The dominant ones, other than the fundamental, are the odd harmonics of order n, where $n = \frac{f_c}{f} \pm 1$ and $n = \frac{f_c}{f} \pm 3$. It can be noticed also that the frequency spectrum of these unwanted harmonics are shifted towards high frequency by

increasing the carrier frequency. In practice, the modulation index is used to control the value of the output voltage of the SPWM inverter. the rms value of the SPWM inverter output voltage as a function of the modulation index at different carrier frequencies, is shown in the following figure
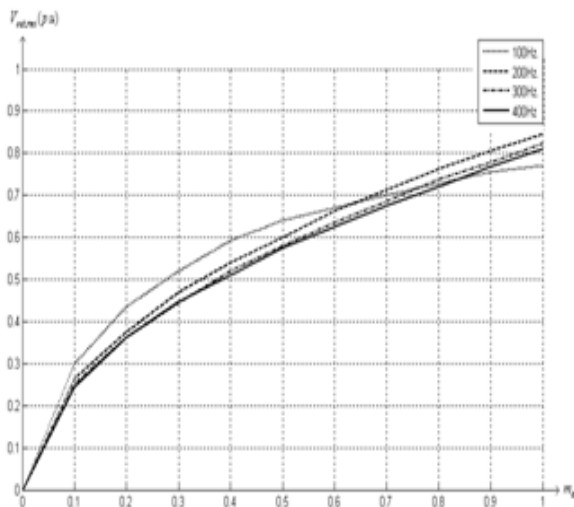

Figure 3: The rms Value of the SPWM Inverter Output Voltage Versus The Modulation Index At Different Carrier Frequencies

The figure below shows the rms value of the fundamental component of the inverter output voltage (in p.u) as a function of the modulation index, at different carrier frequencies.
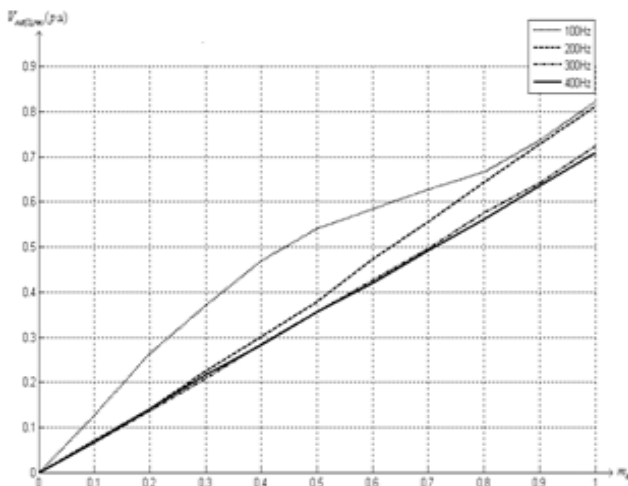

Figure 4: The rms Value of the Fundamental Component of the Inverter Output Voltage (in p.u) Versus the Modulation Index

It comes evident, from the figures below showing the output voltage waveforms of the SPWM inverter that the harmonic contents of the output voltage waveform of this type of inverters is a function of both the modulation index and the frequency of the carrier signal. In other word, both the modulation index and frequency of the carrier signal affect the THD factor of the output voltage waveform of the SPWM inverter. The THD factor as a function of the modulation index at different carrier frequencies is shown in the following figure:
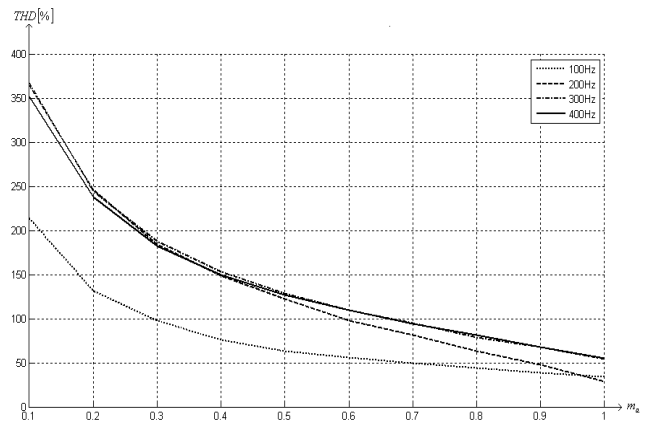

Figure 5: The THD Factor as A Function of the Modulation Index at Different Carrier Frequencies

The THD factor of the output voltage waveform versus the output fundamental voltage is presented in the figure below:
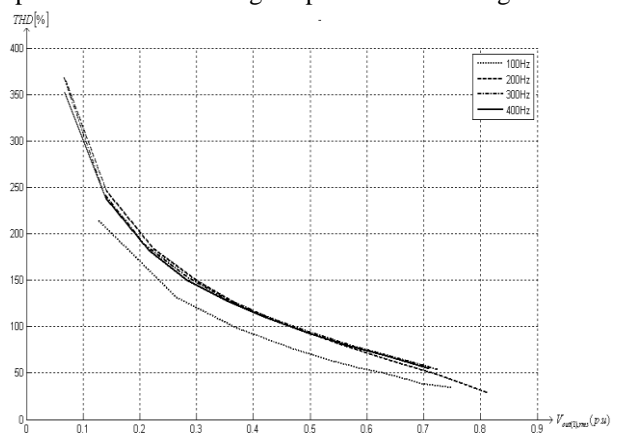

Figure 6: The THD Factor as A Function of the Output Fundamental Voltage, at Different Carrier Frequencies

From these figures, it can be seen that:
- The THD factor decreases as the modulation index, and thus the inverter output voltage, increases.
- For carrier frequencies greater than 400Hz. the THD factor doesn't change much by further increasing the frequency of the carrier signal.
- The THD factor at low values of the modulation index is lower for lower carrier frequencies. However, as known, at lower carrier frequencies, the dominant higher order harmonics are of lower order and the filter required to remove them is larger.

The output voltage waveform of the multi-level voltage source inverter is shaped to be as close to sine wave as possible. This is achieved supplying an H-bridge inverter circuit by a previously determined input voltage levels, at certain switching angles. The harmonic contents of the output voltage waveform of the multi-level inverter are a function of both the voltage levels and the switching angles. The figures below show the output voltage waveforms and the harmonic contents of these waveforms at different number of the voltage levels and different rms values of the fundamental component of the inverter output voltage

From these figures, it can be seen that the dominant harmonics, other than the fundamental, in the output voltage

waveform of this type of inverters are the odd harmonics of order n, where: n=4M+1 and n=4M+3, where M is the number of the DC link stages. It can be also noticed that the frequency spectrum of these unwanted harmonics are shifted towards high frequency by increasing the number of the DC link stages M. The voltage levels of the DC link stages can be used to control the output voltage of the multilevel inverter. The tables below show the voltage levels of the DC link stages and the switching angles versus the rms value of the fundamental component of the inverter output voltage $(V_{out(I),rms})$ in per unit, at different numbers of the DC link stages.

Table 1: The Voltage Level of the DC Link Stage and the Switching Angle Versus the rms Value of the Fundamental Component Of The Output Voltage (V_(out(I),rms)) For A Single-stage (Three-level) Inverter

$V_{out(1),rms}$,[p.u]	0.2	0.4	0.6	0.8	1.0
V_1 , [p.u]	0.256	0.512	0.769	1.026	1.283
α_1 ,[deg]	30	30	30	30	30

Table 2: The Voltage Level of the DC Link Stage and the Switching Angle Versus the RMS Value of the Fundamental Component of the Output Voltage (V_(out(I),rms)) for A Single-stage (eleven-level) Inverter

$V_{out(1),rms}$,[p.u]	0.2	0.4	0.6	0.8	1.0
V_1 , [p.u]	0.080	0.160	0.240	0.320	0.40
V_2 , [p.u]	0.153	0.307	0.460	0.614	0.767
V_3 , [p.u]	0.215	0.429	0.644	0.858	1.072
V_4 , [p.u]	0.258	0.516	0.775	1.033	1.291
V_5 , [p.u]	0.281	0.562	0.843	1.124	1.405
α_1 ,[deg]	8.18^0	8.18^0	8.18^0	8.18^0	8.18^0
α_2 ,[deg]	24.55^0	24.55^0	24.55^0	24.55^0	24.55^0
α_3 ,[deg]	40.91^0	40.91^0	40.91^0	40.91^0	40.91^0
α_4 ,[deg]	57.27^0	57.27^0	57.27^0	57.27^0	57.27^0
α_5 ,[deg]	73.64^0	73.64^0	73.64^0	73.64^0	73.64^0

From the previous tables, the voltage levels of the DC link stages and the switching angles versus the rms value of the fundamental component of the inverter output voltage ($V_{out(1),rms}$), at different numbers of the DC link stages, are shown in the following figures.

From figures above, it can be seen that, in addition to the fundamental component, a set of higher order harmonics are existing in the output voltage waveform of the multi-level voltage-source inverter. The harmonic contents of the output voltage waveform are a function of the number of the inverter DC-link stages. The tables below show THD factor of the inverter output voltage waveform as a function of the rms value of the fundamental component of the inverter output voltage ($V_{out(1),rms}$) at different numbers of the DC link stages.

Table 3: The THD Factor of the Inverter Output Voltage Waveform Versus the rms Value of the Fundamental Component Of The Inverter Output Voltage (V_(out(I),rms)) For A Single-stage (Three-level) Inverter

$V_{out(1),rms}$,[p.u]	0.2	0.4	0.6	0.8	1.0
THD , [%]	31	31	31	31	31

Table 4: The THD Factor Of The Inverter Output Voltage Waveform Versus the rms Value Of The Fundamental Component Of The Inverter Output Voltage V_(out(I),rms)) For A Single-stage (eleven-level) Inverter

$V_{out(1),rms}$,[p.u]	0.2	0.4	0.6	0.8	1.0
THD , [%]	8.25	8.25	8.25	8.25	8.25

The figure below shows the THD factor variations of the output voltage waveform for different numbers of the DC link stages (M).

5. Discussion

The analysis of the SPWM and the multi-level voltage source inverters show that:

- The THD factor of the output voltage waveform of the multi-level voltage source inverter is generally less than that of the SPWM inverter. This means that the multi-level VSI allows, when applied, a relatively cheaper and simpler filtration of the output voltage waveform. For example and for the case of the three-stage inverter, the THD factor of the output voltage waveform is found to be less than 13 %, which is considerably low.
- Increasing the number of DC-link stages means more harmonics can be eliminated, leading to further improvement of voltage waveform quality. However, this is achieved on the expense of more design complexity of the system. The number of stages of the DC link and, hence, the number of harmonics to be eliminated, is a trade-off between the design complexity of the system in one side, and the waveform quality and, hence, the overall system performance in the other side.
- The THD factor of the multi-level VSI is constant for the complete range of the inverter output voltage. This means that the harmonic contents and thus the quality of the output voltage waveform is not varying with the value of the inverter output voltage. This implies that this inverter is suitable for implementation in variable-voltage variable- frequency (VVVF) applications.
- The relation between the value of the fundamental component of the inverter output voltage and of the DC-link voltage levels is linear and is load independent.
- The switching angles are constant for a given frequency of the inverter output voltage. These last two features lead to a relatively simpler control of this type of inverters.

These results demonstrate the attractive features of the multi-level VSI when compared to the conventional SPWM inverters.

6. Conclusion

In this work, the multi-level voltage source inverter is presented. The design features and the principle of operation, of this type of inverters, are reported. The performance of this inverter, and specially the total harmonic distortion (THD) factor, has been analyzed and compared with that of the well-known SPWM inverters

The results found demonstrate the attractive features of the multi-level inverter when compared to other conventional counterparts. Each stage of the DC link provides two degrees of freedom in terms of system controllability, leading to elimination of two harmonic components in the output voltage waveform. The number of undesired harmonics that can be eliminated from the output voltage waveform of the multilevel inverter is directly dependent on the number of stages of the DC link. For an m stage system, it is possible to eliminate 2M-1undesired harmonic components. For example, for the three-stage DC link inverter the first five undesired harmonics can be completely eliminated, leaving the inverter output voltage waveform to be almost sinusoidal with a THD factor to be noticeably low (13%).

The number of DC link stages in the multi-level inverter is a trade-off between the design complexity and the output voltage quality requirements. The THD factor of the multi-level inverter is found to be constant for the complete range of the inverter output voltage. This means that the quality of the output voltage waveform is not varying with the value of the inverter output voltage. This implies that this inverter is suitable for implementation in variable-voltage variable-frequency (VVVF) motor drive applications.

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