Characterizing Standard Cells for Intra-Cell Variations

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Abstract: *Standard cell characterization refers to the process of compiling data about the behavior of the cell. It is necessary to capture accurate values of delay, power and various other characteristics. As the technology is shrinking to satisfy the demand for faster, low-power chips, the impact of small variation in the circuit parameters is increasing exponentially. This variations did not have significant impact on the standard cells of higher nodes. But at lower nodes these have significant impact, which if not considered may lead to design failures. In this paper we discuss a method of characterization where we consider the variation on different parameters of the standard cells and the impact it has on the delay values.*

Keywords: Liberty Variation Format (LVF), Standard cells, Characterization, Global mismatch parameters, Local Mismatch parameters

1. Introduction

A Standard Cell Library contains a collection of logic gates over a range of fan-in and fan-out. Besides the basic logic functions, such as an inverter, AND, OR, NAND, NOR, XNOR and latches and Flip-Flops, they also include more complex functional cells such as Comparator, Multiplexers, Full-Adders and other functionalities as well. The main purpose of using the Standard Cell Libraries in the Semi-Custom Design Flow is to shorten the design process. Among others a high quality standard cell library needs to have accurate data values. Over the time different liberty formats have been developed, each considering various parameter that can effect the cell characteristics. A .lib contains timing and power information among other data which is accumulated using characterization tools with circuit simulator. Earlier models did not consider the impact of variations in the parameters of the standard cells. Butas the technology is shrinking, the impact of the variation on the characteristic of the standard cells has increased. On technology above 20nm this variations did not have significant impact on the cells. Thus there was little need for considering the impact of variations. But at lower nodes we can observe significant deviation in the delay parameters of the cell for small variations. These variations can arise during the manufacturing process like the lithography among others stages. This variations can be change in the channel length, the width of the channel, the oxide thickness. This variations in turn will have significant impact on the mobility and the threshold value of the cells which in turn has impact on the speed of the cells.

The variations are broadly classified into *Global* and *Local* variations. Typically the wafer to wafer, across wafer, and chip to chip variations are called Global variations or inter-chip variation. Where as the variation across a chip is called local variation on intra chip variations.

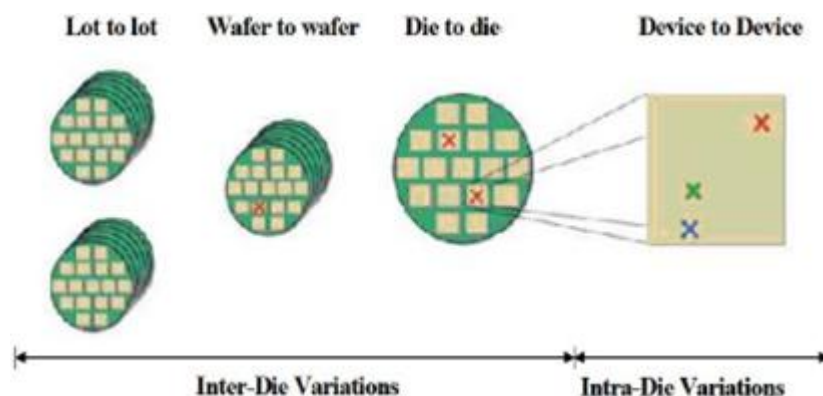The fig 1 below shows the global and local variations.

Figure 1: Process variations [1]

As can be seen in the Fig 1 the global variation is regarded as the deviation in the mean or the expected value across a die. Where as the local variations is within a chip or a cell. In this paper we will be considering intra-cell mismatch parameters. The Fig 2 shows an example where the variation to each transistor of the NAND gate is applied independently.
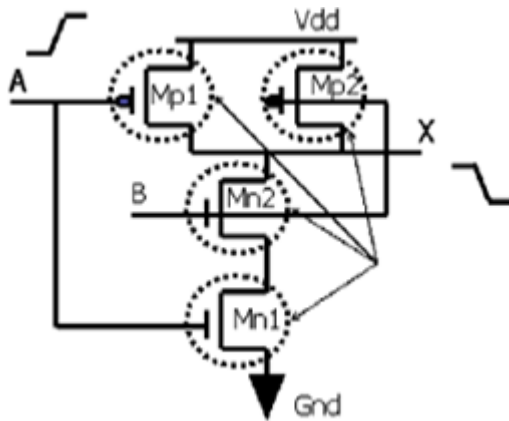
Figure 2: Intra cell variation [2]

2. Methodology

In this paper statistical Characterization flow is adopted. The Statistical variation gives the spread of values from there mean value. Here the cells are characterized for variation in delay, transition and the constraints (setup, hold, recovery and removal) due to process variation.
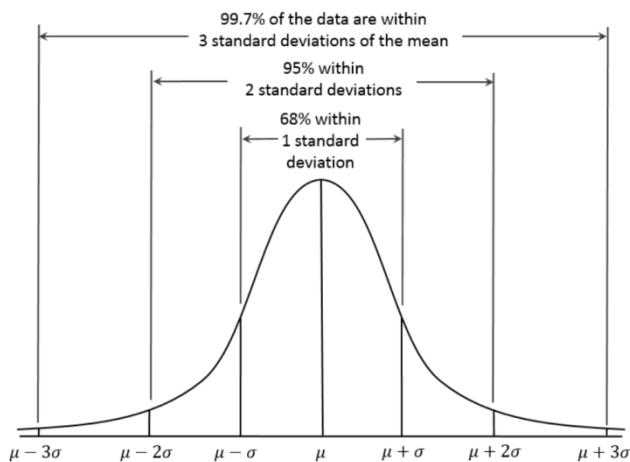

Figure 3: Cell Delay Variation

The delay distribution due to variation is in the form of Gaussian distribution as shown in Fig 3. As can be seen, considering a deviation of 3-sigma gives a delay spread of around 99.73% which is sufficient for modeling.

To understand statistical flow its important to understand how sensitivity and sigma values are calculated.
Consider an inverter with one PMOS and one NMOS.

Consider 5 process parameters per transistor: np1, np2, ….,np5 for NMOS and pp1, pp2, ..., pp5 for PMOS, for a total of ten individualparameters. The delay equation for any process parameter combination is expressed as shown in equation 1

$$D = D0 + s1 \cdot \Delta np1 + s2 \cdot \Delta np2 + … + s6 \cdot \Delta pp1 + … \quad (1)$$

Where D0 represents the nominal delay, s1,s2,….s6 refers to sensitivity values, $\Delta np1$, $\Delta np2$…. $\Delta pp1$ are changes in the parameters

The sensitivity values s1, s2, etc… are found through simulation by varying one process parameter at a time, per transistor.
Assuming that the distribution of the delay D is Gaussian, the standard deviation of D is given by equation 2

$$\delta = \sqrt{s1^2 \cdot \delta1^2 + s2^2 \cdot \delta2^2 + … + s10^2 \cdot \delta10^2}$$

where

$\delta1$, $\delta2$, ..., are the standard deviations of $np1$, $np2$, ...

Characterization flow
The inputs required for the characterization tool are transistor level netlist, instance file, config files. To generate the LVF liberty model for NAND gate first a layout of NAND gate was constructed, from which transistor level netlist was extracted. From the PDK the local mismatch parameter associated with each of the transistor models used in the NAND gate needs to be identified and specified.

Specifying the MOSFET names.

```
set pmos_model_names { pch_mac }
set nmos_model_names { nch_mac }
```

Specifying the local variation parameters associated with each of the transistors
add_opc_statstical_parameter FF -intracell para1 -model { nch_macpch_mac }

where para1 is one of the local parameter associated with the nmos and pmos transistors. Now due to variation in this parameter across the cell the delay value will deviate from its mean value, which would be more significant at lower voltages. Depending upon how much variation is expected in this parameters its sigma value is defined, that will be the max sigma value the parameter is varied from its mean value. These parameters are independently varied between the sigma values and the deviation for a particular timing arc is generated. Fig 4 shows the siliconsmart flow for generation of liberty files.
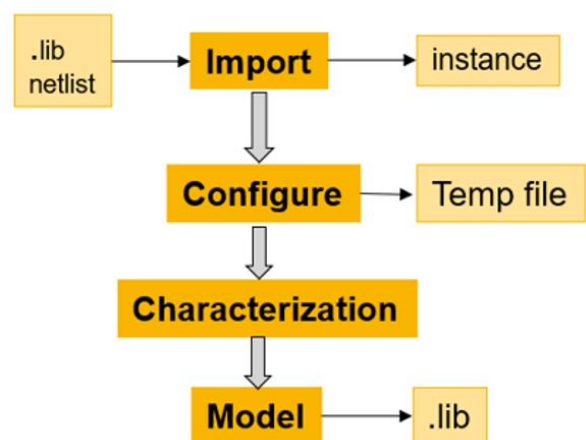

Figure 4: Siliconsmart data flow

3. Implementation and Results

Figure 5: Layout of NAND gate

The Fig5 shows the layout of the NAND gate. After creating the layout netlist is extracted from the layout which is then given to the characterization tool for generation of the .lib
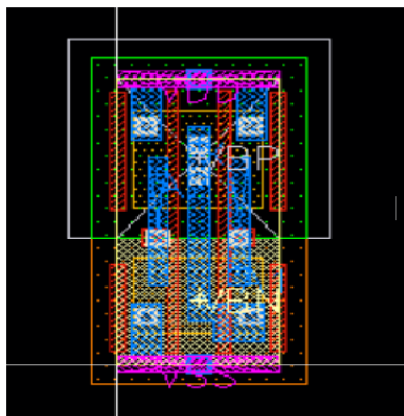

Figure 6: Liberty file

Fig 6 shows a part of the .lib in which the variation in delay for *early* and late is shown. For each timing arc *late* and *early* tables are generated which shows the deviation in the timing values. Here we can see that in "sigma early" for the slew value of 0.002 and the load value of 0.00017 the delay value obtained is 0.0296047 and the variation in delay at the early side is 0.00297947 which is around 10% of its value.

4. Conclusion

At lower technologies the delay of the standard cells is less, thus the impact of the variation on the standard cell results in the magnitude of the deviation values in timing being significant percentage of the original delay values. At even lower technology the deviation will be even more significant. This when not considered during the RTL-GDSII flow may lead to design failures.

References

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