Electrical Properties of Radio-Frequency Sputtered HfO_2 Thin Films for Gate Dielectric Application

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Abstract: ***Hafnium oxide (HfO_2) high-k thin films have been deposited by radio frequency (rf) sputtering technique on p-type Si (100) substrate. The thickness, composition and phases of films in relation to annealing temperatures have been investigated by using cross sectional FE-SEM (Field Emission Scanning Electron Microscope) and grazing incidence x-ray diffraction (GI-XRD), respectively. GI-XRD analysis revealed that at annealing temperatures of 350 ^{0}C, films phases change to crystalline from amorphous. The capacitance-voltage (C-V) and current-voltage (I-V) characteristics of the annealed HfO_2 film have been studied employing Al/HfO_2/p-Si metal–oxide–semiconductor (MOS) structures. The electrical properties such as dielectric constant, interface trap density and leakage current density have been also extracted from C-V and I-Measurements. The value of dielectric constant, interface trap density and leakage current density of annealed HfO_2 film is obtained 23,$7.57\times10^{11}eV^{-1}$ cm^{-2} and 2.7×10^{-5} Acm^{-2}, respectively. In this work we also reported the influence of post deposition annealing onto the trapping properties of hafnium oxide and optimized conditions under which no charge trapping is observed into the dielectric stack.***

Keywords: High-k, HfO_2, FE-SEM, C-V

1. Introduction

High-k dielectric materials have been developed as alternative gate oxides to overcome the scaling limit of conventional Si-based insulators due to high tunnelling and reliability concerns. Among the various high-k dielectrics materials such as Al_2O_3[1]-[2],HfO_2[3],TiO_2[4],CeO_2[5], $LaAlO_3$ [6], HfSiO [7], ZrO_2[8], HfO_2 has emerged as one of the most promising materials for its high dielectrics constant, high density, large bandgap, low density of interface states and a good thermal stability in contact with silicon relative to the other high-k materials. Since high-k gate oxides play vital role in constitution of a MOS structures, extremely high quality and well controlled thin films growth are essential. A number of various film growth techniques can be employed to fabricate HfO_2 thin films such as thermal oxidation [9], molecular beam-epitaxy (MBE), atomic layer deposition (ALD)[10]-[12], chemical vapor deposition (CVD)[13], pulsed laser deposition (PLD), DC and RF sputtering[14]. Among them, radio frequency (RF) sputtering explores the possibility of obtaining the good quality high-k gate dielectric thin films required in advanced CMOS technology for its several advantages such as high deposition rate at low temperature, good uniformity, and also the ability to deposit compact films with high stability. The defects and impurities present in the film can be reduced by post deposition annealing (PDA) with improving the dielectric constant during structural modifications.

In this study, HfO_2 thin films were deposited by RF sputtering on p–type Si (100) substrate. The structural characteristic of grown thin films was investigated by XRD, FE-SEM in a more detailed manner to understand the effect on the grown film's properties of physical growth conditions. The electrical properties of Al/HfO_2/p-Si MOS structure were obtained through high-frequency Capacitance - Voltage (C-V), Conductance-Voltage (G-V) techniques and Current -Voltage (I-V) measurement.

2. Experimental Details

The starting materials are $2''$ p-type Si wafers 〈100〉 with a resistivity of about 1-20 Ω/cm. were cleaned using standard RCA cleaning. This Si wafers then loaded in RF sputtering system for the deposition of HfO_2 thin films immediately after standard RCA cleaning. Prior to sputtering the chamber was vacuumed to 4×10^{-6} mbar, ionized argon was then pumped into the chamber. HfO_2 thin films were deposited by 99% pure HfO_2 ceramic target. The process parameters like operating pressure, sputtering distance, sputtering time and sputtering power for the deposition of HfO_2 thin films were set as 0.018 mbar, 4.8 cm, 50 min and 150 W, respectively at room temperature. Before each deposition, the HfO_2 target was pre-sputtered for 5 min at 75 W for cleaning purposes and then depositions were run at 150 W. To study both the bulk and interface properties, relative thicker films (of about 20 nm) were used, despite this thickness is much larger than that used in the current technology node. The post deposition annealing of the as-deposited films was performed in oxygen ambient (Ar and O_2 flow) for 40 min at 350 °C temperature without breaking the vacuum condition. The Al metal has been deposited as top metal electrode on HfO_2 thin films through shadow mask by using Thermal evaporation system (Model No.-12A4D) at base pressure of 2×10^{-5} mbar where substrate temperature was kept at room temperature. Crystal structures of the films and thickness were examined using a Philips X'Pert X-Ray Diffract meter (XRD) with Cu Kα radiation at 1.54 Å and cross-sectional FE-SEM, respectively. The Al is also deposited on backside of Si substrate for formation of ohmic contact to form MOS capacitors by thermal evaporation technique. Capacitance as a function of voltage, *C–V* and current as function of voltage, *I–V* (keithley 4200 SCS) measurements of these fabricated Al/HfO_2/Si MOS structures were performed to extract the various electrical parameters.

3. Results and Discussion

3.1 Structure Studies

Fig.1 (a) & (b) show the scanning electron micrograph of the HfO_2 thin film annealed at 350 ^{0}C. The thickness of the film was 20 nm. The thin film exhibits a cross-section with 20 nm thick and a surface with very fine granule texture. The GI-XRD measurement was carried out to investigate the structure of the HfO_2 thin film annealed at 350 ^{0}C (Fig. 2). The peak from (111) crystal plane be the most intense one, which is consist with the powder diffraction data of monoclinic HfO_2.

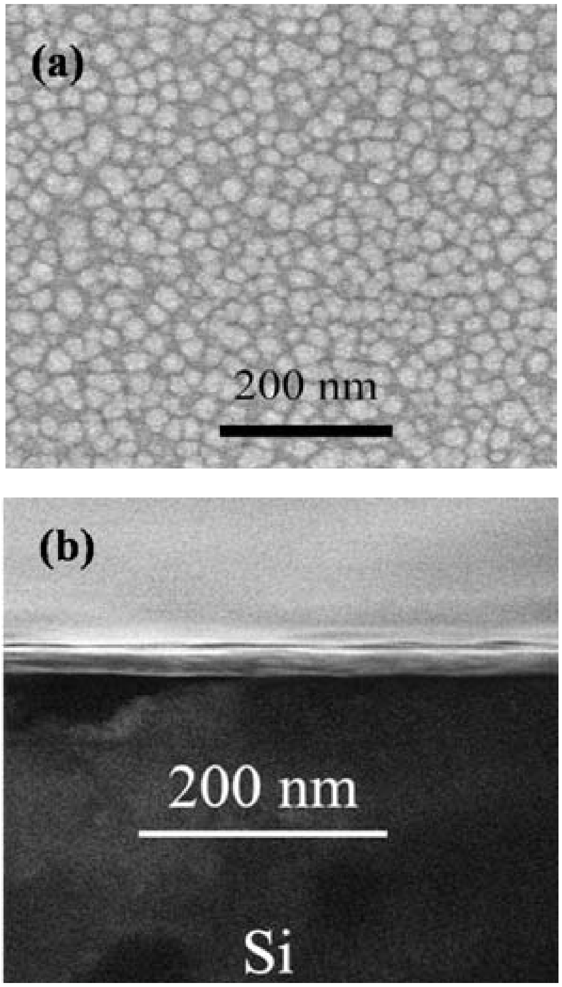

Figure 1(a) and (b): Surface and cross-section morphologies of HfO_2 thin film annealed at 350 ^{0}C

3.2 Capacitance–Voltage characteristics

Typical *C-V* characteristics curves of MOS structure at different frequencies of the sample annealed at 350 ^{0}C are shown in Fig. 3 which clearly shows accumulation, depletion and inversion regions. The dispersion observed in the accumulation region is due to the substrate series resistance *R*s, which mainly affects the high-frequency *C–V* curve [15], series resistance R_s is determined to be 736.22 Ω at 1 MHz frequency. Hysteresis effect in high frequency *C–V* curves is observed as shown in Fig. 3 When *C–V* curve is traced from inversion to accumulation region inversion capacitance is always lower in both high and low frequency cases. This is attributed to the facts, trap states are not localized only at the interface but could also spatially distributed in the dielectric closer to the interface and interface state shows the non-equilibrium behaviour. Since minority carriers are responsible for the formation of inversion layer and thus it is affected by the generation of minority carriers through interface traps.

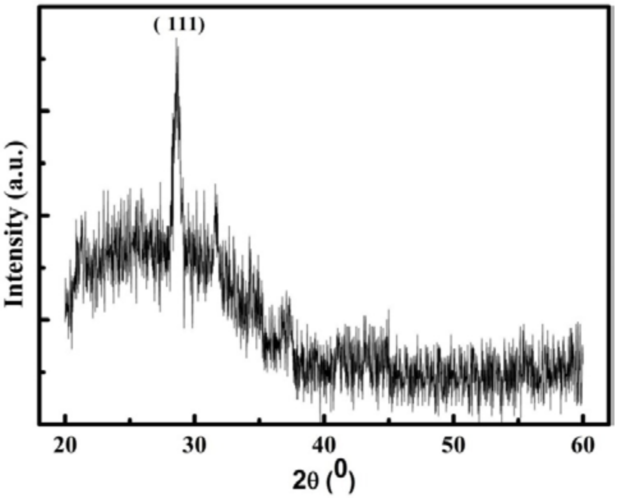

Figure 2 : XRD pattern of HfO_2thin film annealed at 300 ^{0}C

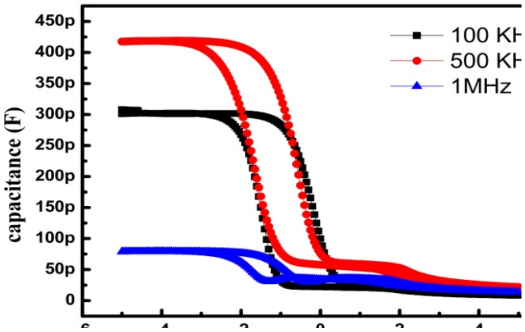

Figure 3: C–V characteristics of the HfO_2 thin film at different frequency

Fig. 4 shows a comparison of the *C–V* curves obtained for HfO_2 films annealed at 350 ^{0}C with as deposited sample (RT) at 1 MHz frequency. In the *C–V* curve the maximum capacitance value in accumulation region was observed to be reduced with annealing temperature. This may be attributed to the absence of interfacial layer between Si and HfO_2. An interface layer would have a lower dielectric constant than the dielectric constant of HfO_2 [16], [17], [18] and [19]. As a result, the overall gate stack capacitance of the MOS capacitor would be lower. The dielectric constant (*k*) value of sample annealed at different temperatures was extracted from the accumulation level of a *C–V* curve and was calculated using the following equation -

$$k=(t_{ox}\cdot C_{ox})/(A\cdot\varepsilon_0) \qquad (1)$$

where t_{ox} is the thickness of oxide layer, $C_{ox.}$ is the accumulation value of capacitance, *A* is the electrode area and ε_0 is the permittivity of free space.

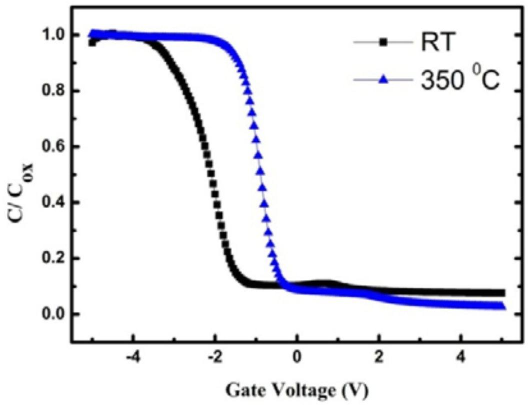

Figure 4: C–V characteristics of Al/HfO2/p-Si MOS capacitors annealed at 350 °C temperatures as deposited sample (RT).

The C-V measurements indicated a dielectric constant of 23 for HfO_2 films annealed at 350 ^{0}C. From the *C–V* curve, negative flat band shift has been observed in all samples. This shift indicates the existence of a large amount of positive effective oxide charge (Q_{eff}) in the HfO_2 layer. The flat band voltage V_{FB} is measured to be −3.5 V for the sample annealed 350 ^{0}C. Assuming that the average charge distribution located at the bottom of interface of the film [20], the effective charge carriers were calculated by the following equation [21]-

$$Q_{eff}=(\Delta V_{FB}\cdot C_{ox})/(q\cdot A) \qquad (2)$$

where C_{ox} is the oxide capacitance, q is the electronic charge and ΔV_{FB} is the flat band voltage shift. The obtained Q_{eff} for samples annealed at 350 °C is 97.44 × 10^{-9} C/cm^{-2}. Fig. 5 shows conductance–voltage (*G–V*) curve at 1 MHz frequency. The density of interface states (D_{it}) was calculated from the Conductance–Voltage characteristics by the Hill-Coleman method [22]. The value of D_{it} estimated at 1 MHz frequency is 7.57 × 10^{11} eV^{-1}cm^{-2}.

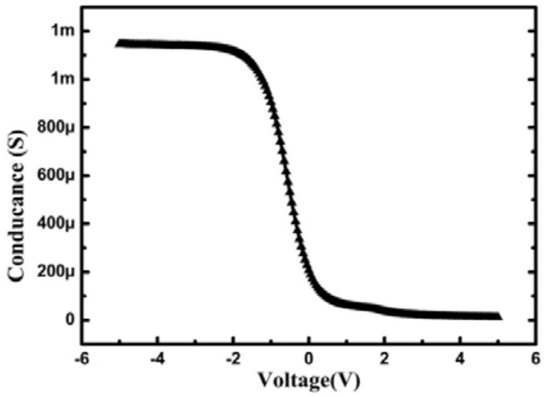

Figure 5: Conductance–voltage curve of Al/HfO2/Si MOS capacitor with annealed HfO_2 thin film

3.2 Current–Voltage characteristics

A typical leakage current density (J-V) characteristic of the investigated samples annealed at 350 ^{0}C with RT is shown in Fig. 5. The leakage current density of devices with 350 ^{0}C annealed HfO_2 film is 2.7 × 10^{-5} A/cm^{-2} at 3 V, which is lower than the leakage current density of as-deposited sample.

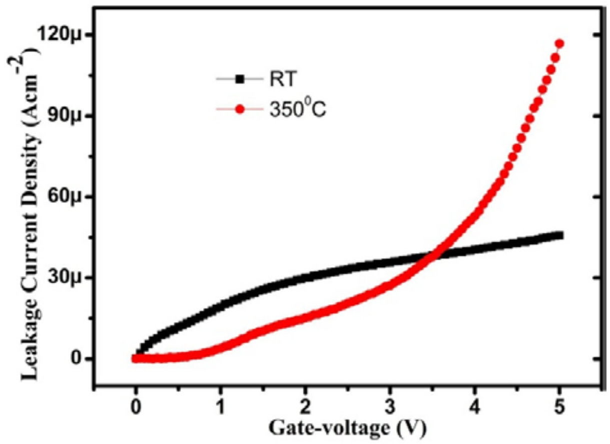

Figure 8: J-V characteristics of Al/HfO2/p-Si MOS capacitor annealed at 350temperatures with as-deposited sample

4. Conclusion

In this work, HfO_2 thin film with thickness of 20 nm was successfully deposited on Si substrate by rf sputtering. Samples were annealed in oxygen ambient. Physical and electrical characterizations of the HfO_2thinfilm MOS capacitor with post deposition annealed at 350 ^{0}C temperatures were studied. The electric properties like effective oxide charge Q_{eff} (97.44 × 10^{-9} C/cm^{-2}), density of interface traps D_{it}(7.57 × 10^{11} eV^{-1}cm^{-2}), and lowest leakage current density (2.7 × 10^{-5} A/cm^{-2} at 3V) holds good electrical reliability from the C-V and I-V curves obtained for fabricated Al/HfO2/p-Si MOS capacitors.

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