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Design and Performance Comparison of finFET, CNFET and GNRFET based 6T SRAM

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Abstract: ***Static Random Access Memory (SRAM) has long been the way to store electronic data on-chip, in high speed circuits. The myriad of low area, high speed ICs are the consequence of advent in MOSFET scaling techniques. A disquisition on Limits on MOSFET scaling reveals a need for new transistor technology. The paper provides three SRAM (6T) cell models (Graphene Nano-ribbon FET, Multi-walled CNT FET and MOSFET) which paves the way for technology comparison. The parameters such as Read delay, Write delay and Power-delay product are considered. For all the three technologies, 10nm gate length is used. Design of a complete SRAM cell is then considered (6T SRAM cell, Precharge circuit, Sense amplifier, Read and Write circuits) to provide power comparison between 32X8, 32X16, 64x8 and 64x16 SRAM arrays. Circuit design and simulation was done using HSpice and CosmosScope.***

Keywords: SRAM, Read delay, Write delay, Power-delay product, CNT FET, Graphene Nano-Ribbon FET.

1. Introduction

The advent of high performance VLSI chips require a cutting edge method to store electronic data, on chip to meet performance needs. SRAMs are the pinnacle of such solutions. SRAMS are a critical part of a wide range of microelectronic devices. Consumer demand advocates a reduction in size of memory storage devices. With advances in scaling growing, new limitations are introduced on use of sub 10nm MOSFETs in very large-scale integrated (VLSI) circuit design, such as sensitivity to process variations and increase in transistor leakage. Scaling has reached a critical apogee where the leakage currents have become a major setback. Such results demand a new FET technology altogether. A genial response to such demands was provided by the advent of graphene.

1.1 Graphene

Single layered Graphene, an exfoliated alloy of carbon, emerged as a promising solution in 2004, as the first two dimensional material with striking electronic, magneto-electronic and optoelectronic properties. Due to high mobility ballistic transport, fast state switching due to extremely high carrier mobility and electrostatic reduction due to the 2D structure, Graphene based devices have a promising future in supplanting conventional CMOS nano electronics. The mobility of exfoliated Graphene was reported to be 100,000 cm2 V^{-1} s^{-1} (On insulated substrates) [1] and 230,000 cm2 V^{-1} s^{-1} for suspended structures [5].Graphene exhibits a thermal conductivity of 5300 W m-1 K-1at room temperature [3].The first entry of Graphene into FET was in 2007. The paper uses Graphene Nano-Ribbon (GNR) FETs. The prospect of band gap engineering in GNR propels the material for extensive future use in nano-electronic circuits due to its exotic characteristics such as large carrier mobility and planar structure.

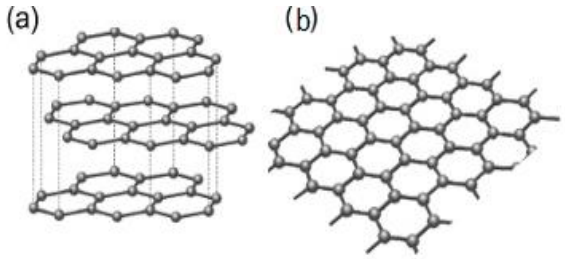

Figure 1: (a) Graphite represented in multiple sheets **(b)** Exfoliated Graphene.

1.2 Carbon Nano-Tubes

Carbon Nano Tubes (CNT) was discovered by SumioIjima [2] in 1991. Single walled CNTs (SWCNT) are formed by rolling single graphite sheets to produce a cylindrical structure. The carrier mobility of SWCNTs were proved to be around 80000 cm2V-1s-1 [3]. CNTs have an electric capacity 1013A m-2 [6]. The thermal conductivity of CNTs at room temperature was shown t be 3500 W m-1 K-1 [7]. Out of the two types of CNTs (single walled multi walled), the paper utilizes multi walled CNTFETs. CNT offers an extremely high carrier velocity of 1X108 cm/s. CNTs today are grown on wafers achieving up to 99% and upwards of alignment [8]. Performance of a CNT-FET exceeds that of a conventional Silicon transistor, as evidenced by Javey et al [6]. Some applications of CNTs are electron source in field emission devices, interconnects and FETs. The presence of

an intrinsic band-gap is the main reason for to build CNT FETs. CNT-FETs have their conducting channel made of CNTs.

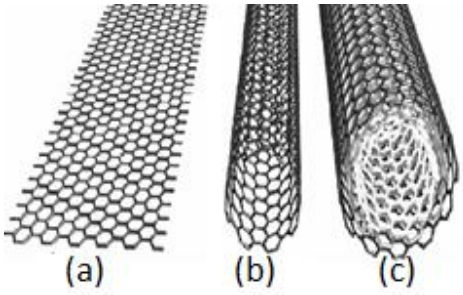

Figure 2: (a) Graphene sheet, **(b)** Single walled CNFET, **(c)** Multi Walled CNFET

1.3 finFET

FinFET is double gated MOS device which gives superior performance because they are less susceptible to short channel effects and can be built using standard bulk planar CMOS processing. They are practical candidates for analog as well as digital applications and are considered to be one of the best candidates for sub-65 nm scaling of silicon MOSFETs.

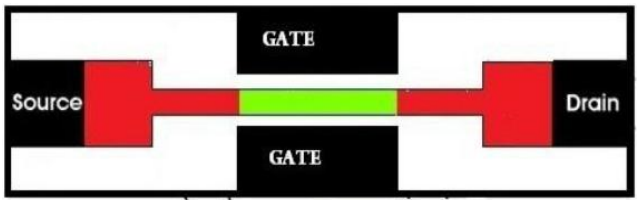

Figure 3: Top view of finFET

Fig. 3 shows the structure of multi-fin double-gate FinFET devices. Double gate FinFET consists of two SOI gates connected together. The thickness (T_{si}) of a single fin equals to silicon channel thickness. The current flows from the source to drain along the wafer plan. Each fin provides 2H of device width, where H is the height of the each fin. For the FinFET devices, widths are quantized into units of the fins. Large width of device is obtained by using multiple fins.

1.4 SRAM Cells

A typical six transistor (6T) SRAM cell is shown in Fig. 1. in a 6T SRAM cell, storage nodes are directly accessed through the pass transistors connected to the bit lines. The storage nodes are disturbed due to the voltage division between the cross-coupled inverters and the access transistors during a read operation[10]. The robustness of an SRAM cell is characterized by the hold stability during read operation as the data is most vulnerable to external noise during a read operation, due to intrinsic disturbance produced by the direct data-read-access mechanism (destructive read)[9].

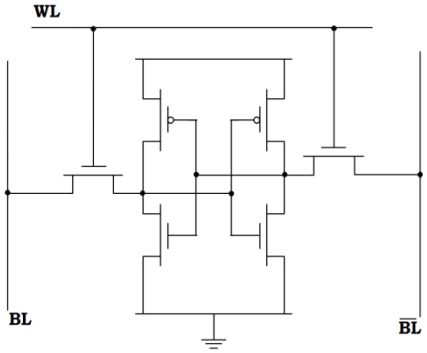

Figure 4: 6T SRAM cell: WL – word line, BL – bit line.

There are strict constraints on the sizing of transistors to be able to maintain the data stability and functionality of a standard 6T SRAM cell as shown in Table 1. The design of a 6T SRAM cell is typically characterized by the ratio (β) of the size of the pull-down transistors to the access transistors. In order to maintain the read stability, N1 and N2 must be stronger as compared to the access transistors N3 and N4. Alternatively, for write ability, N3 and N4 must be stronger as compared to P1 and P2. These requirements are satisfied with careful transistor sizing, as illustrated in Fig.4

2. Conventional 6T SRAM, a functional overview

A conventional 6T SRAM comprises of 6 transistors designed simply to form two cross coupled inverters placed back-to-back. This cell is used to either store a single bit data or read a single-bit data from the cell[11]. When a bit is stored, the SRAM works as a latch. The small leakage currents of both the CMOS inverters contribute towards the total leakage power consumption of the memory cell[13]. The use of cross coupled inverters leads to a slightly larger area consumption; which is a drawback as compared to the resistive load and depletion load NMOS SRAM Cell. The memory cell consists of a simple CMOS latch in which two inverters connected back-to-back and two complementary access transistors M1 and M2[12, 14,15]. As long as the power supply is available, the cell will preserve one of its two possible states. Conventional SRAM cell with 6T is shown in figure 4. There are mainly three states in SRAM cell the write, read and hold states[16,17]. In the following paragraphs, we describe the states a conventional 6T SRAM cell:

2.1 Data Hold State

When WL = “0”, M1 and M2 disconnect the cell from bit lines (Bit and Bit bar). The current drawn in this state from the Vdd is termed as leakage current.

2.2 Data Read State

Read operation starts with pre-charging Bit and Bit bar to high. Within the memory cell M3 and M6 are ON. Asserting the word line, turns ON the M1 and M2 and the values of Q and Q' are transferred to bit-Lines. No current flows through M2, thus M2 and M6 pull Bit bar up to Vdd, i.e., Bit bar = “1” and Bit line discharges through M1 and M3. This voltage difference is sensed and amplified to logic levels by sense amplifiers [18].

2.3 Data Write State

The value to be written is applied to the bit lines and keep WL="1". Thus to write data "0", we assert Bit=0, Bit bar= "1" and to write data "1", the Bit = "1", Bit bar ="0".

2.4 Write delay

It is the delay between the applications of the word line WL signal and the time at which the data is actually written.

2.5 Read Delay

Read delay is the delay involved in allowing the bit lines to discharge by about 10% of the peak value or the delay between the application of the WL signal and the response time of the sense amplifier.

3. Work done and Results

The work was focused mainly on analysis of access - time and power dissipation.

Initially, finFET, CNTFET and GNRFET based 6T single bit SRAM was designed using 10nm transistor gate length and the dissipated power was calculated for all the designs using HSpice. Later, to validate the results obtained, higher order 6T SRAMs (32X8, 32X32, 64X8 and 64X16) were designed and power analysis was done using HSpice tool.

3.1 Power Dissipation of Single Bit SRAM

GNRFET based single bit 6T SRAM cell dissipates least power, about 23.46 µW, as compared to that by CNT-FET based design which dissipates 284.3µW and finFET based SRAM design which dissipates 30.6µW. Power dissipation of single bit SRAM Cell is as shown below in Fig. 5.

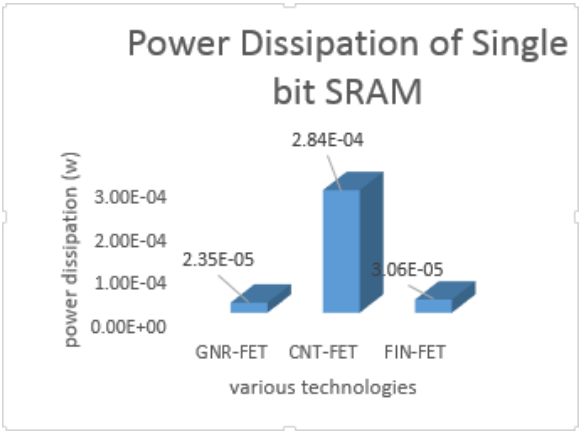

Figure 5: Single Bit SRAM Power Dissipation

3.2 Read and Write Delays

Speed of operation of SRAM varies with the technology used, due to the disparate intrinsic characteristics of the technologies themselves. The read and write delays (Read-1, Read-0, Write-1, Write-0) of a single bit SRAM designed using GNRFET, CNT-FET and finFETs are as shown in the fig. 6

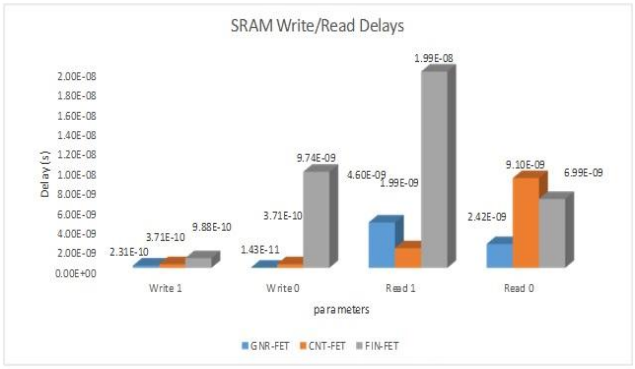

Figure 6: Read and Write delays

The Fig. 3.2 clearly depicts GNR-FET based 6T SRAM to be the frontrunner in terms of speed, while writing onto the cell. Writing to the cell involves charging or discharging the inverter inside the cell. Physical characteristics of the MOSFETs such as sheet resistance, drain current decides the celerity in charging or discharging the cell. Different set of characteristics pivot the delay encountered while reading from a cell. Carbon nano-tube devices show a greater drain current than graphene based or finFET based devices, for the same gate voltage and channel length. Therefore CNT-FET based devices outperform the GNR-FET and finFET counterparts while charging the same capacitive load. On the contrary, while reading a '0' from the cell, the worst case delay implies discharging an already charged bit-line. Graphene based transistors, boasting a lower sheet resistance, perform better in this case, and followed by finFETs and CNT-FET based devices.

3.3 Power Parameter of multiple cell SRAMs:

The results of 6T 1-bit SRAM clearly depicts that GNRFET based single bit 6T SRAM design, in the big picture, outperforms that by CNTFET and finFET based designs. In order to validate the work for extended architectures, 32X8, 32X32, 64X8 and 64X16 6T SRAM arrays were designed using finFETs, CNTFETs and GNRFETs and their performance was analysed. In all the four architectures, GNRFET based design dissipates least power as compared to finFET and CNTFET based designs due to its higher mobility and current carrying capacity, low thermal conductivity as well as least sheet resistance. The highest measured sheet resistance and a comparatively higher drain current of SWCNTs acts as the major contributor to the elevated power dissipation of CNTFET based design, among the three designs and in all the architectures. Fig. 7,8,9,10 are the graphs comparing the power dissipation of the various 6T SRAM architectures.

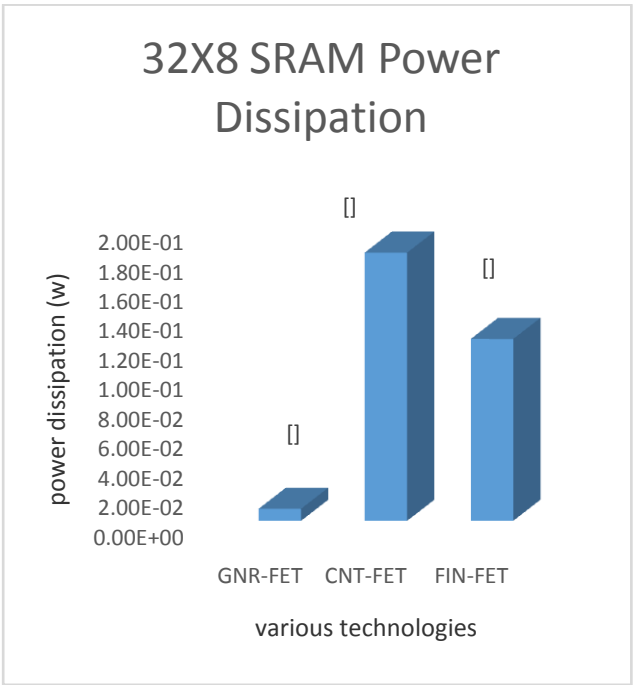

Figure 7: 32X 8 SRAM Power Dissipation

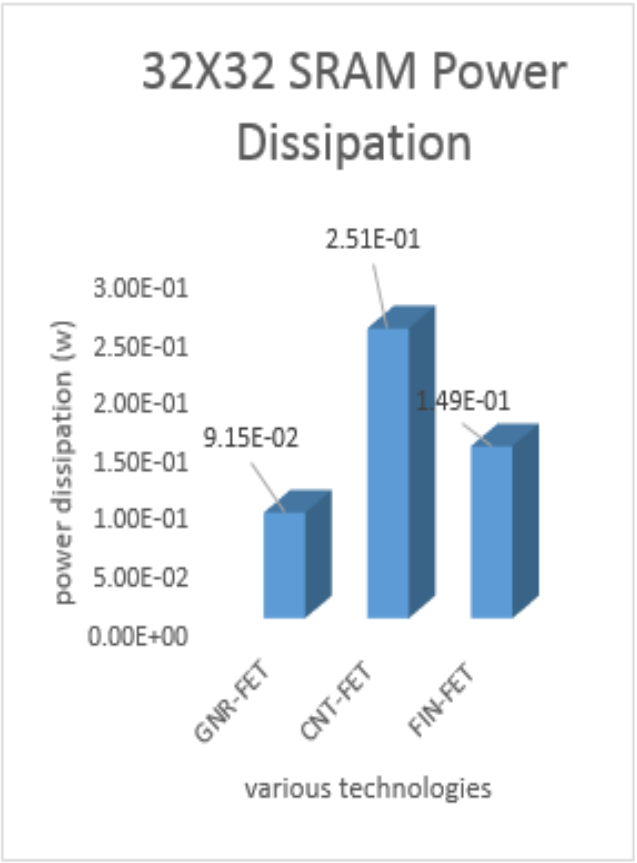

Figure 8: 32X 32 SRAM Power Dissipation

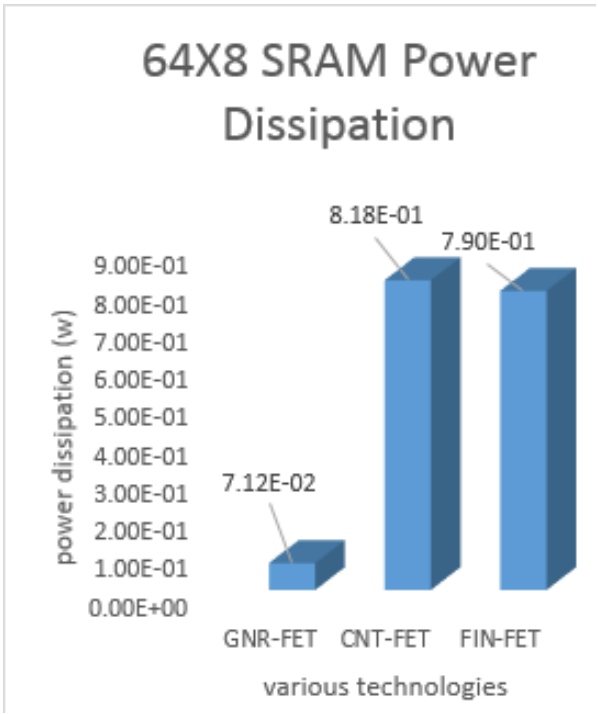

Figure 9: 64X 8 SRAM Power Dissipation

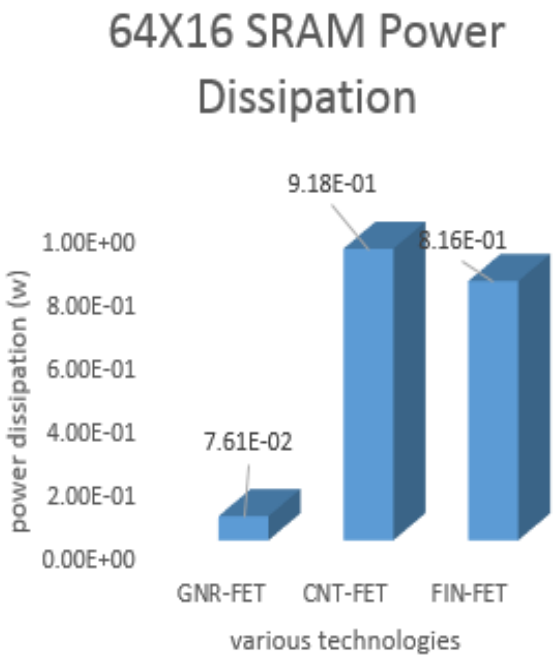

Figure 10: 64 X 16 SRAM Power Dissipation

4. Conclusion

Our work here aims at providing a proven solution to the ever increasing demand for higher memory capacity, bogged down by the woes of increasing power dissipation, with increased demand for scaling, leading to adverse short channel effects. We provide multiple designs whose performance parameters such as Power dissipation, access times are compared over multiple design architectures. The bird's eye view depicts the CNT-FET based designs as having the highest power dissipation amongst the three designs, in all architectures. On an average, the GNRFET

based designs dissipated around 10x less power than its CNT-FET and finFET counterparts, which proves Graphene based devices to be a superlative choice to combat power dissipation, with increased scaling. The different designs provide a varied performance over access times measurement. GNRFET based design shows the least write delay amongst the three designs, whereas CNT-FET based design performs marginally better while writing onto the bit line. Both GNRFET and SWCNT-FET based designs outperform the silicon FET based design while still providing a future for further scaling.

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