

A New Structure of Asymmetric Multilevel Converter with Increased Number of Output Voltage Levels

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Abstract; *This paper deals with asymmetric multilevel converter with a single source that can produce greater amount of output voltage waveforms with a reduced number of power electronic components. The power electronic switches play a very important role in designing a multilevel converter because they define the cost, installation area, circuit size and complexity. MOSFETs are used as switches. The existing system of asymmetric cascade topology significantly increases the number of output voltage levels. The main function of multilevel converter is to remove total harmonic distortion and to synthesize desired ac voltage from several separate dc sources. Each level consists of H-bridge converter units. It has the advantage of high efficiency, high voltage capability, lower switching losses, etc. A multilevel power converter structure can be introduced as an alternative in medium voltage and high power situations. This structure not only achieves high power ratings but also enables the use of renewable energy sources. It finds its basic application in adjustable speed drives, Static Var Compensator (STATCOM).*

Keywords: Asymmetric, Multilevel Inverter, SVM, Cascaded H-Bridge

1. Introduction

The concept of multilevel converter came into the mind of researchers in 1975[1]. The multilevel converters can act as both a converter and an inverter. They can produce large number of output voltage levels with high voltage capability. The multilevel converters have more than two output voltage levels with respect to a reference point. The term multilevel began with the three level converters. For a medium voltage grid, it is difficult to connect only one power semiconductor switch directly. Thus, a multilevel power converter introduces an alternative in high power and medium voltage situations [2]. concept of a multilevel converter to achieve high power is use to semiconductor switches with several lower voltage dc sources to perform the power conversion. A multilevel converter has several advantages over a conventional two level converter that uses high switching frequencies pulse width modulation (PWM) [3].

- i. Staircase waveform quality: The converter not only generates output voltage with low distortion but also low dv/dt stress.
- ii. Common-mode (CM) voltage: The converters produce smaller common mode voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. The common mode voltage can be eliminated using the advanced modulation strategies.

- iii. Input current: Multilevel converter can draw input current with low distortion

- iv. Switching frequency: The converters can operate at both fundamental switching frequency and high switching frequency PWM. Multilevel converters also have some disadvantages. The greatest of them is the requirement of greater number of semiconductor switches [4]. Lower voltage rated switches can be utilized, but each switch will require a related drive circuit. This can increase the overall complexity and cost of the system. In general, there are three types of multilevel converters: 1) Neutral Point Clamped (NPC); converter 2) Flying Capacitor (FC) converter; 3) Cascade H-Bridge (CHB) converter. The main drawback of NPC converter is the unequal voltage sharing among series connected capacitors. Moreover, this structure needs large number of clamping diodes for higher levels[7]. Contrary to this, the FC converter requires large number of storage capacitors for higher output voltage levels and capacitor voltage balancing is difficult. Conventional cascade multilevel converter is the most important amongst the used topologies because it requires least number of components [8]. A cascaded converter comprises of H-bridge cells. The major drawback is that it requires large number of isolated dc supplies. This can increase the overall complexity of the system. So, to overcome it, split On the basis of configuration, the converters can be divided as symmetric, asymmetric and cascaded form multilevel converter [10]. multilevel converter uses dc sources of similar values, while asymmetric multilevel converter uses dc sources of unequal values. The cascaded multilevel converter uses the

configuration of either symmetric or asymmetric multilevel converter. Numerous studies have been made by the researchers for the control on multilevel converter. They can be different on the basis of configura[11]. For asymmetric multilevel converter, voltagevector approximation technique is applied, which is a type of fundamental frequency control. Whereas for symmetric multilevel converter, both low switching and high switching frequencies are considered. These approaches include space vector modulation, multicarrier PWM strategy, amplitude control and harmonic reduction.

2. Proposed 19 Level Asymmetric Multilevel Converter.

The block diagram below shows the proposed work of asymmetric multilevel converter.

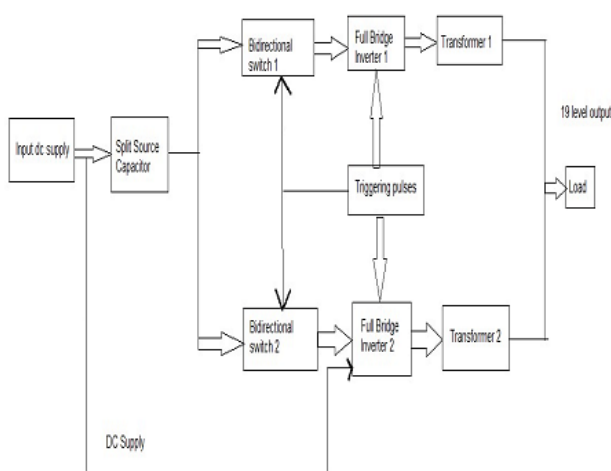


Figure 1. Block Diagram of 19 Level Asymmetric Multilevel Converter

The proposed system of asymmetric multilevel converter consists of a single dc source. The asymmetric multilevel converter provides an increased number of output voltage levels for the same number of power electronic devices when compared to its symmetric counterpart. It should be noted that a multilevel converter can act both as an inverter and a rectifier. The cascaded H-Bridge topology is used to get the desired number of levels. Each switch is comprised of H-bridge cells. Each block of switches is provided with a triggering pulse. The major disadvantage of cascaded H-bridge cells is that it requires greater number of isolated dc sources in the input side. The greater number of dc sources can increase the complexity of the circuit and cost. To minimize this complexity, split source capacitors are used. The main function of these capacitors is to equally divide the input voltage source amongst the power electronic switches. The methodology used in the multilevel converter is the space vector modulation technique.

3. Methodology

The space vector PWM technique is an algorithm for control of pulse width modulation. It is commonly used

to drive 3 phase ac powered motors at varying speeds from dc using multiple Class D amplifiers. One active area of development of SVM is in the reduction of total harmonic distortion (THD) created by rapid switching inherent to these algorithms (figure 2). An inverter is commonly used in variable speed AC motor drives to produce a variable, three phase, AC output voltage from a constant DC voltage. Basically, amplitude and frequency defines the two characteristics of AC voltage. Thus it is essential to work out a strategy on how to control both these quantities [13]. With a three phase voltage source inverter there are eight possible operating states. In (figure 4), the upper switch of the inverter’s pole A is on whereas the lower switch is off. Contrary to this, on the other two legs, the upper switch is off while the lower switch is on for V (100) condition.

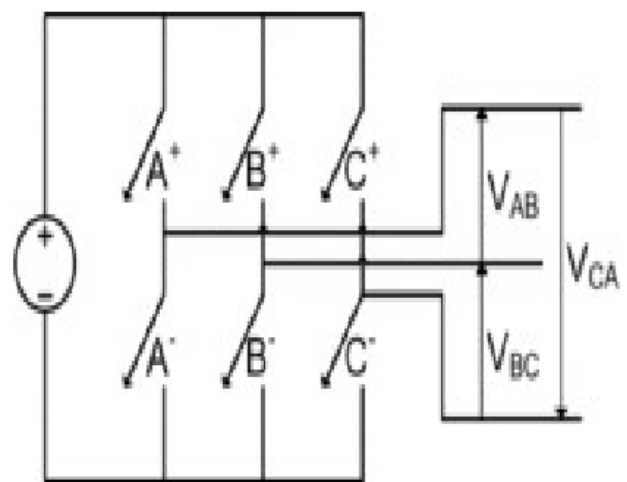


Figure 2. Topology of a Basic Three Phase Inverter

Because of the constraint that the input lines must never be shorted and the output current must always be continuous a voltage source inverter can assume only eight distinct topologies. Six out of these eight topologies produce a non-zero output voltage and are known as non-zero switching states and the remaining two topologies produce zero output voltage and are known as zero switching states.

The space vector modulation (SVM) for three-leg VSI is based on the representation of the three phase quantities as vectors in a two-dimensional plane. This can be seen in the vector representation diagram. The voltages V_{Vca} are three line voltage vectors displaced by 120degrees in space. plane. This can be seen in the vector representation diagram. The voltages V_{ab} , V_{bc} and V_{ca} are three line voltage vectors displaced by 120.

4. Experimental setup

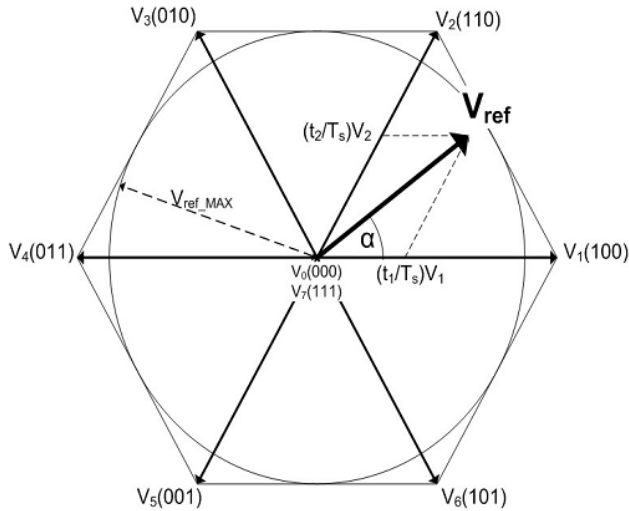


Figure 3. Vector Representation of SVM

The diagram below shows the circuit diagram of the proposed system. The input dc source of 90 V is used. A total of nine split source capacitors are used. The main function of split source capacitor is to equally divide the input source to the switches. MOSFETs are used as the switches with the desired three phase voltages at the output of the inverter could be represented by an equivalent vector V_{ref} . The reference vector is then synthesized using combination of two adjacent active switching vectors and one or both of the zero vectors. combination of diodes with it. A total of thirty two diodes are used. Also twelve MOSFET switches are used. A subsystem designated as “Out1” is used to provide the pulses to the gate of MOSFET and input to the triggering pulses block. The diodes are such connected that they are anti parallel to each other. Some of the MOSFET switches are individually used and the pulses are given through the subsystem interconnected to it. The voltage measurement and current measurement blocks are also used for ideal voltage and current measurement respectively. Series RL branch is also used to obtain the desired output. Finally the output is taken from the output voltage parameter. Combination of diodes with it. A total of thirty two MOSFET switches are used. A subsystem designated as “Out1” is used to provide the pulses to the gate of MOSFET and input to the triggering pulses block. The diodes are such connected that they are anti parallel to each other. Some of the MOSFET switches are individually used and the pulses are given through the subsystem interconnected to it. The voltage measurement and current measurement blocks are also used for ideal voltage and current measurement respectively. Series RL branch is also he desired output. Finally the output from the output voltage parameter.

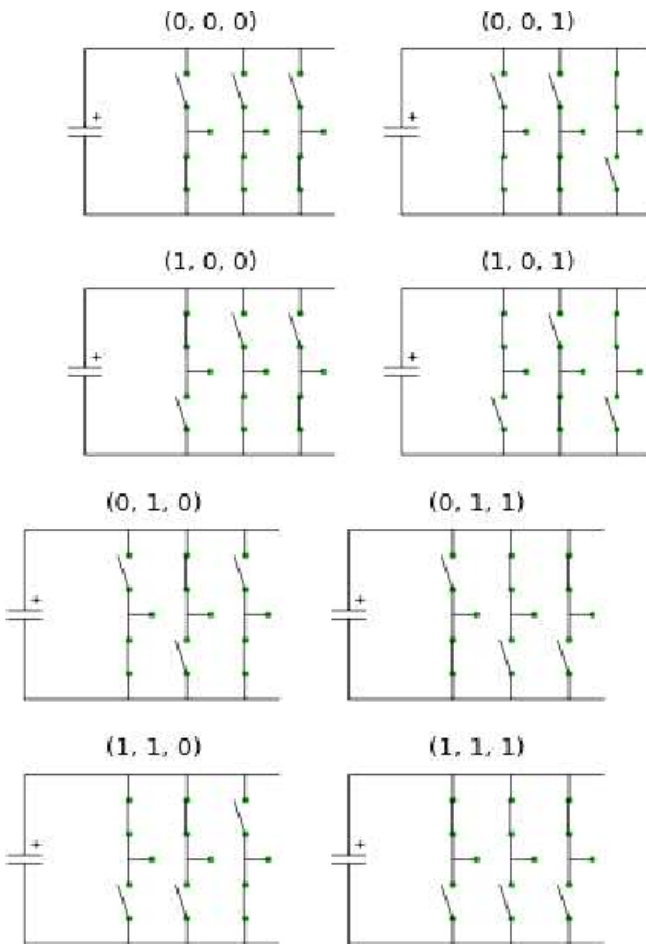


Figure 4. Eight possible Switching States

The magnitude of this vector is related to the magnitude of the output voltage and the vector takes to complete one revolution is the same as the fundamental time period of the output voltage.

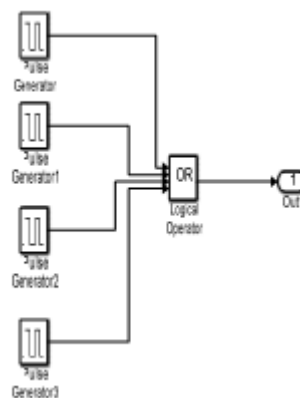


Figure 5. Subsystem of Generating Pulses

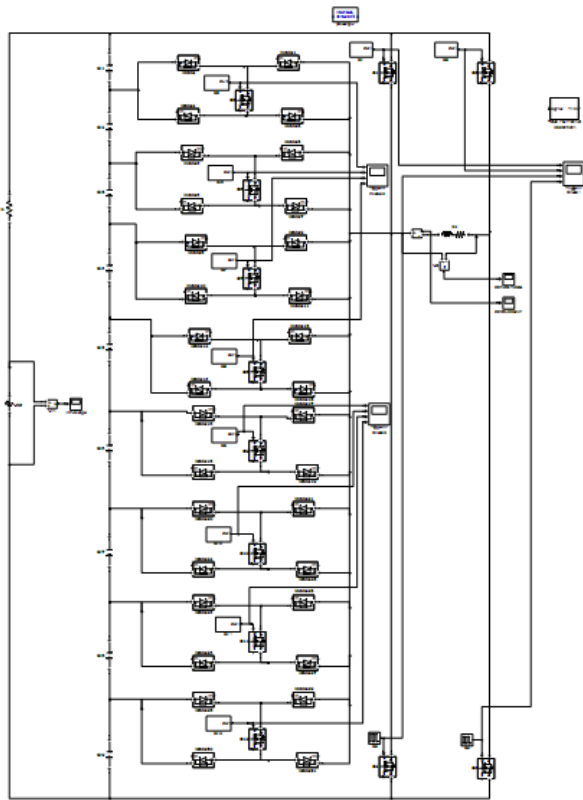


Figure 6. Circuit Diagram of Proposed System

5. Simulation Results Simulation Results

This section deals with the simulation results of the proposed 19 level asymmetric multilevel converter. Single dc source of value 90V is used as the input source. The value of output voltage frequency is 50Hz.

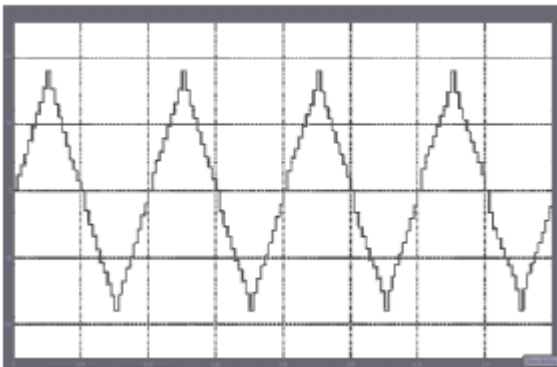


Figure 7. Output Voltage Waveform

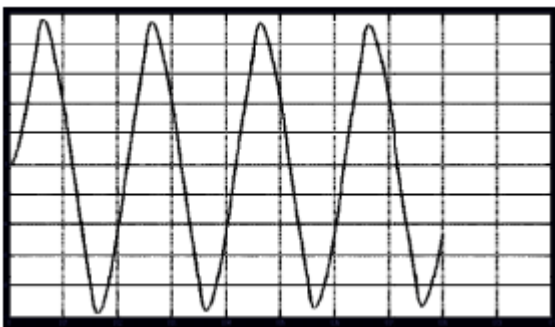


Figure 8. Output Current Waveform

The proposed system uses thirty two diodes with a combination of twelve MOSFETs as switches. For this case, the THD of the output voltage based on simulation is 5.70%. The efficiency of the converter is based on the applied control strategy. This paper uses fundamental frequency control strategy. Thus the efficiency of the converter is high.

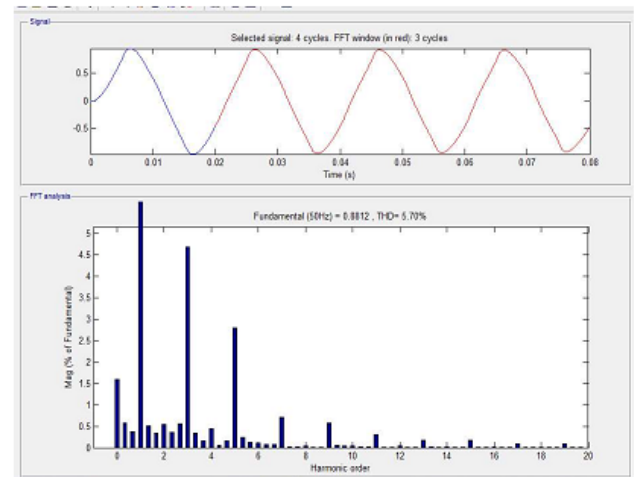


Figure 9. Harmonic Spectrum (THD 5.70%) Harmonic Spectrum (THD 5.70%)

6. Conclusion

This paper proposes a new structure for asymmetric multilevel converter. This new structure minimizes the use of dc source and also increases the output voltage waveform. This system is suitable for medium and high voltage applications. Because of the use of single dc source and less number of switches, the overall cost and complexity of the system is reduced. The fundamental frequency control strategy increases the efficiency of the converter.

7. References

- [1] Rasoul Shalchi Alishah, Daryoosh Nazarpour, Seyed Hossein Hosseini, “Novel Topologies for Symmetric, Asymmetric and Cascade Switched Converter with Minimum Number of Power Electron Components”, IEEE Transactions on Industrial Electronics, Vol. 61, no. 10, October 2014, pp 5300
- [2] Surin Khomfoi, Leon M. Tolbert, “Chapter Power Converters”, the University of Tennessee, Publication: EECS, 2007, pp 1-50
- [3] Valery Vodovozov, Raik Jansikene, “Power Electronic Converters”, Publisher Tallinn: TUT, 2006, pp 1
- [4] Mohammad N. Abdul Kadir, Saad Mekhilef, Hew Wooi Ping, “Dual Vector Control Strategy for a Three Stage Hybrid Cascaded Multilevel Inverter”, Journal of Power Electronics, Vol. 10, no. 2, March 2010, pp 155
- [5] E. Babaei, M. T. Haque, S. H. Hosseini, “A

Novel

Structure for Multilevel Converter”, Electrical Machines and Systems, 2005, ICEMS, 2005, Proceedings of Eighth International Conference (Vol. 2), pp 1278

[6] M. N. Abdul Kadir, S. Mekhilef, H. W. Ping, “Voltage

Control of Three Stage Hybrid Multilevel Inverter Using Vector Decomposition”, Power Electronics, IEEE Transactions on Vol. 3, no. 4, 2010, pp 601-611

[7] Madhav D. Manjrekar, Peter K. Steimer, Thomas A. Lipo,

Hybrid Multilevel Power Conversion System: A Competitive Solution for High Power Application”, IEEE Transactions on Industry Applications, Vol. 36, no. 3, May/June 2000, pp 834-841

[8] R. A. Ahmed, S. Mekhilef, H. W. Ping, “New Multilevel

Inverter Topology with Reduced Number of Switches”, in Proc. Int. Middle East Power System Conf., 2010, pp 565-570

[9] Y. S. Lai, F. S. Shyu, “Topology for Hybrid Multilevel

Inverter”, Proc. Int. Elect. Engg.-Elect. Power Appl., Vol 149, no. 6, November 2002, pp 449-458

[10] N Khader Basha, M Abid Nayeemuddin, “A New

Cascaded multilevel Inverter with Less Number of Switches”, International Journal of Research in Engineering and Technology, pISSN: 2321-7308, Vol.

2, Issue 9, September 2013, pp 159-165

[11] Rokan Ali Ahmed, S. Mekhilef, Hew Wooi Ping, “New

Multilevel Inverter Topology with Less Number of Switches”, Proceedings of 14th International Middle East

Power Systems Conference (MEPCON’10), Cairo University, Egypt, December 19-21, 2010, Paper ID 236, pp 565-570

[12] Hulusi Karaca, “A Novel Topology for Multilevel Inverter

with Reduced number of Switches”, Proceedings of World Congress on Engineering and Computer Science (WCECS) 2013, Vol. 1, October 23-25, 2013, San Francisco, USA, pp 350-354

[13] Implementing Space Vector Modulation with the ADMCF32X, © Analog Devices Inc., January 2000, pp 1-22