

Design and Analysis of Two-Stage Op-Amp in 0.25μm CMOS Technology

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Abstract: In this paper, the detailed study of Op-Amp and its characterizing parameters is presented. Parameter measurements of a Two-stage Op-Amp are presented along with measurement set-ups and simulation results. The design of a Two-stage Op-Amp is done to perform various parameter measurements. A two-stage Op-Amp is designed in 0.25μm CMOS technology. The designed Op-Amp operates at 2.5V power supply. The Op-Amp achieves 61.5 dB of Open-loop gain, 64° phase margin, Gain Bandwidth of 31 MHz, 20 KHz of 3-dB Cutoff frequency, 10V/μs of Slew rate with 0.82mW power consumption.

Keywords: Op-Amp, Two-stage Op-Amp, parameters of an Op-Amp, measurements of Op-Amp parameters.

1. Introduction

In the design of analog circuits the tradeoff among the various parameters such as power dissipation, speed, supply voltage, noise performance etc. is observed. To design an optimum analog system, the multi-dimensional optimization is necessary [1]. The functioning of the analog system depends on the accuracy of sub-systems used to build the system. As in most of the analog systems, an Op-Amp is used as a basic building block. Therefore, the design of a stable optimized Op-Amp is necessary. The parameters that characterize the performance and stability of Op-Amp must be known numerically, so that optimization can be performed with high accuracy. The different analyses performed to determine the characteristics of an Op-Amp are DC, AC, Transient, and Noise analysis with different stimulus [1],[2].

In this paper, section II gives the basic idea of an Op-Amp. Different topologies of Op-Amp and there comparison are given in section III. Basic parameters that characterize an Op-Amp, globally, are presented in section IV. Various parameter measurement set-ups are presented along with the simulation results in section V. finally, conclusions are drawn in section VI.

1. Operational Amplifier

An Op-Amp (Operational Amplifier) is a high gain differential amplifier. Ideally an Op-Amp is characterized by an infinite open-loop gain (A_{∞}), Infinite input resistance ($R_{in}=\infty$), Zero output resistance ($R_{out}=0$), Infinite differential gain ($A_d=\infty$), zero common mode gain ($A_c=0$), infinite bandwidth (BW_{∞}), infinite CMRR (common mode rejection ratio) and infinite SR (slew rate). But practically, there are finite values of these parameters of an Op-Amp [1],[3].

Basically an Op-Amp has two input terminals i.e. Inverting terminal and Non-inverting terminal and one output terminal and power supply. An inverting terminal is one, in which the applied input produces out of phase output.

No-inverting terminal produces in-phase output for applied input.

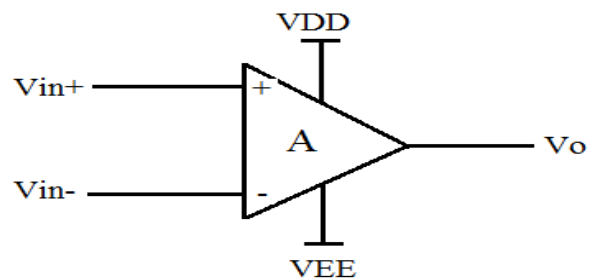


Figure. 1: Basic Op-Amp Symbol

The Basic symbol for an Op-Amp is shown in fig.1 where V_{in+} and V_{in-} are non-inverting and inverting terminals, respectively. V_o is the output terminal and V_{DD} and V_{EE} represent the positive and negative power supplies respectively.

The output of an Op-Amp is given by

$$V_o = A * V_{in} = A * (V_{in+} - V_{in-}) \quad (1)$$

As the Open-loop gain (A) of an Op-Amp is very high about 10^4 to 10^6 . Therefore, Op-Amp is designed to operate in feedback mode [3].

A CMOS Op-Amp is basically a multistage amplifier. It consists of three stages viz.

1. Differential Amplifier stage
2. Gain stage
3. Buffer stage

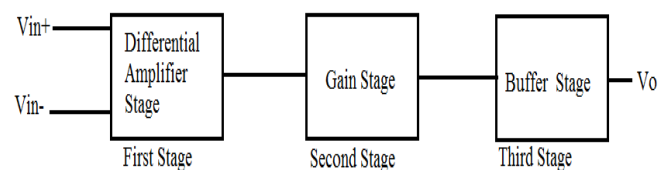


Figure.2: Basic Stages of CMOS Op-Amp

2.1 Differential Amplifier stage: The first stage is a differential amplifier. It provides at the output a differential

voltage or a differential current that, essentially, depends on the differential input only it is the dual-input, balanced-output differential amplifier stage. Here dual input single ended differential amplifier stage is used. This stage generally provides most of the voltage gain of the amplifier and designed so that it provides a high input impedance, large common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), low offset voltage, low noise and high gain.

2.2 Gain stage: In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by second stage which is basically a common source amplifier stage.

2.3 Buffer stage: The last stage is output buffer. It provides the low output impedance and larger output current needed to drive the load of Op-Amp. It normally does not contribute to the voltage gain. If Op-Amp is the internal component of switched capacitor circuit, the output load is usually a capacitor and the buffer need not provide large current or very low output impedance. However, if the op-amp is at the circuit output, it may have to drive a large capacitor and low resistive load. This requires large current driving capability and very low output impedance, which can only be attained by using large devices with appreciable dc bias currents. This is usually a push-pull complementary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of the Op-Amp. A well-designed output stage also provides low output resistance.

In the CMOS Op-Amp when the Op-Amp is used with all three stages it can be operated with resistive loads. But if only capacitive loads are used then only first two stages of an Op-Amp are required and it is called OTA (operational trans-conductance amplifier) [2],[3].

2. Operational Amplifier Topologies

An Op-Amp is the most widely used analog device. There are a number of variants of Op-Amp used for different applications. Most widely used topologies are

- 3.1 Two-stage Op-Amp
- 3.2 Folded Cascode Op-Amp
- 3.3 Telescopic Op-Amp
- 3.4 Gain-boosted Op-Amp

3.1 Two-Stage Op-Amp: - A two-stage Op-Amp is designed with transistors operating in saturation region for all time. It is the simplest approach to realize an Op-Amp. A two stage Op-Amp has advantage of having high differential output voltage swing. The output voltage swing (V_{swing}) for a two stage Op-Amp is given by

$$V_{swing} = 2V_{sup} - 4V_{ds,sat} \quad (2)$$

Where V_{sup} = supply voltage and

$V_{ds,sat}$ = minimum required voltage to saturate a transistor.

A two-stage Op-Amp operates at relatively low frequency signal as to shift the non-dominant pole and consumes high power.

3.2 Folded-Cascode Op-Amp:- In the two-stage Op-Amp only $V_{ds,sat}$ is needed to saturate the bottom-most load

transistor and top-most current source transistors. In order to allow a process variation, a small safety margin (V_{margin}) is often added to $V_{ds,sat}$ to ensure saturation. The output voltage swing (V_{swing}) for a folded cascode Op-Amp is given by

$$V_{swing} = 2V_{sup} - 8V_{ds,sat} - 4V_{margin} \quad (3)$$

Although, the currents in the output stage can be much smaller than that flowing through the input devices, in practice, the output stage current is picked to be the same or almost the same as the current in the input stage.

Folded cascode amplifiers has better frequency response than two-stage Op-Amp whereas having two extra legs requires settling requirement and hence increases power consumption.

3.3 Telescopic Op-Amp: - A Telescopic cascode amplifier has better noise and power performance, which makes it a better candidate for low power low noise single stage operational trans-conductance amplifier it has small output voltage swing that limits the dynamic range. The differential output voltage swing (V_{swing}) is given by

$$V_{swing} = 2V_{sup} - 10V_{ds,sat} - 6V_{margin} \quad (4)$$

In most of the analog circuits, telescopic Op-Amp is not a good choice because the performance parameters of Op-Amp with no tail and with tail, transistors in the linear region is sensitive to most common mode and supply voltage variation.

3.4 Gain-Boosted Op-Amp: - The limited gain of a single stage Op-Amp and low frequency response of two-stage Op-Amp requires the design of high gain Op-Amp. Also the Telescopic Op-Amp and Folded Cascode Op-amp used to attain high gain by maximizing the output impedance using additional cascade stages and increase the power consumption [1],[3].

In order to attain high gain without adding cascade stages the Gain-Boosted Op-Amp is used.

Table.1 Comparison of various topologies

Topology	Gain	Output Swing	Speed	Power Dissipation	Noise
Two-Stage	High	Highest	Low	Medium	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Telescopic	Medium	Medium	Highest	Low	Low
Gain-boosted	High	Medium	Medium	High	Medium

4. Parameters of Operational Amplifier

An Op-Amp can be characterized by a number of parameters. Some of important parameters are as follow

4.1 Open-loop gain (A_{DC}): - Operational Amplifiers are mainly used to amplify the input signal. Higher the open-loop gain better the performance of Op-Amp and has lower non-linearity. The open-loop gain of Op-Amp, in most applications, is adjusted by using in feedback mode. Ideal

Op-Amp has infinite gain. For practical Op-Amps, the gain is finite. Typical values for low frequency and small signals are 10^2 - 10^5 , corresponding to 40-100 dB [5]-[6].

4.2 Input impedance, (Z_{in}): - The Input impedance of an Op-Amp for an ideal device has to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry.

4.3 Bandwidth(BW): - An ideal operational amplifier has an infinite Frequency Response and can thus be used to amplify signals of any frequency. However, it is observed from the AC analysis of the Op-Amp the frequency response curve below the gain of the amplifier is not constant irrespective of frequency and after the first pole it begins to drop with a slope of 20dB/decade thus the higher the frequency of the first pole the higher the range of frequencies over which it operates desirably.

4.4 Finite Linear Range: - The linear relation in equation 1 between the input and output voltages are valid only for a limited range of V_o. Normally the maximum value of V_o for linear operation is somewhat smaller than the positive dc supply voltage, the minimum value of V_o is somewhat positive with respect to the negative voltage.

4.5 Offset Voltage: The amplifiers output is supposed to be completely independent of common potentials applied to both inputs and is supposed to be zero when the voltage difference between the inverting and non-inverting inputs is zero.

For an ideal Op-Amp, if V_{in+} = V_{in-} (which is easily obtained by short circuiting the input terminals) then V_o = 0. In real devices, this is not exactly true, and a voltage V_{o,off} ≠ 0 will occur at the output for shorted inputs. Since V_{o,off} is usually directly proportional to the gain, the effect can be more conveniently described in terms of the input offset voltage V_{in,off} defined as the differential input voltage needed to restore V_o = 0 in the real devices. For MOS op-amps V_{in,off} is about 5- 15mV.

4.6 Common Mode Rejection Ratio (CMRR): The common-mode input voltage is defined by V_{in_c} = (V_{in+} + V_{in-})/2 as contrasted with the differential-mode input voltage V_{in_d} = V_{in+} - V_{in-}. The differential gain A_D and also the common-mode gain A_C which can be calculated as

$$A_D = \frac{V_o}{V_{in_d}} \quad (5)$$

$$A_C = \frac{V_o}{V_{in_c}} \quad (6)$$

The CMRR is now defined as the ratio of differential gain to the common mode gain and it can be expressed in dB. The expression for CMRR are given as

$$CMRR = \frac{A_D}{A_C} \quad (7)$$

$$CMRR_{dB} = 20 \log \left(\frac{A_D}{A_C} \right) \quad (8)$$

Typical CMRR values for MOS amplifiers are in the 60-80 dB range. The CMRR measures how much the op-amp can suppress common-mode signals at its inputs. These normally represent undesirable noise, and hence a large CMRR is an important requirement.

4.7 Unity Gain Bandwidth: - Because of stray capacitances, finite carrier mobilities and so-on, the gain A_{DC} decreases at high frequencies. It is usual to describe this effect in terms of the unity gain bandwidth, that is the frequency f₀ at which |A_{DC}(f₀)| = 1. For MOS op-amps, f₀ is usually in the range of 1-10 MHz. It can be measured with the op-amp connected in a voltage-follower configuration.

4.8 Slew Rate:- For a large input step voltage, some transistors in the Op-Amp may be driven out of their saturation regions or completely cut-off. As a result the output will follow the input at a slower finite rate. The maximum rate of change output voltage with respect to time is called slew rate. It is not directly related to the frequency response. Mathematically slew rate is given by

$$SR = \frac{dV_o}{dt} \quad (9)$$

For typical MOS op-amps slew-rates of 1-20 V/μs can be obtained

4.9 Nonzero Output Resistance:- For a real MOS Op-Amp, the open loop output impedance is nonzero. It is usually resistive, and is of the order of 0.1-5KΩ for Op-Amps with an output buffer, it can be much higher (~1MΩ) for Op-Amps with un-buffered output. This affects the speed with which the Op-Amp can charge a capacitor connected to its output and hence the highest signal frequency.

4.10 Noise: - The MOS transistor generates noise, which can be described in terms of an equivalent current source in parallel with the channel of the device. The noisy transistors in an Op-Amp give rise to a noise voltage V_{O,noise} at the output of the Op-Amp, this can be again modeled by an equivalent voltage source V_{noise} = V_{O,noise}/A_{DC} at the Op-Amp input. Unfortunately, the magnitude of this noise is relatively high, especially in the low frequency band where the flicker noise of the input devices is high; it is about 10 times the noise occurring in an Op-Amp fabricated in bipolar technology. In a wideband (say in the 10Hz to 1MHz range), the equivalent input noise source is usually of the order of 10~50μV RMS, in contrast to the 3~5μV achievable for low-noise bipolar Op-Amps [1]-[4],[11]-[14].

5. Simulation Results

In the design of Operational Amplifier, to determine the various characteristics, a number of analyses are performed. Some of the analyses are presented here. The analyses are performed on simple two-stage Op-Amp designed in 0.25μm CMOS technology.

A two-stage Op-Amp schematic diagram is shown in fig.3 [8]-[10],[15]. And the corresponding symbol generated for the two-stage op-Amp of fig. 3 is shown in fig.4.

Table 5.1 shows the transistor sizes used for two-stage Op-Amp. Here the minimum length is 0.5µm which is greater than 0.25µm due to allowance of fabrication process.

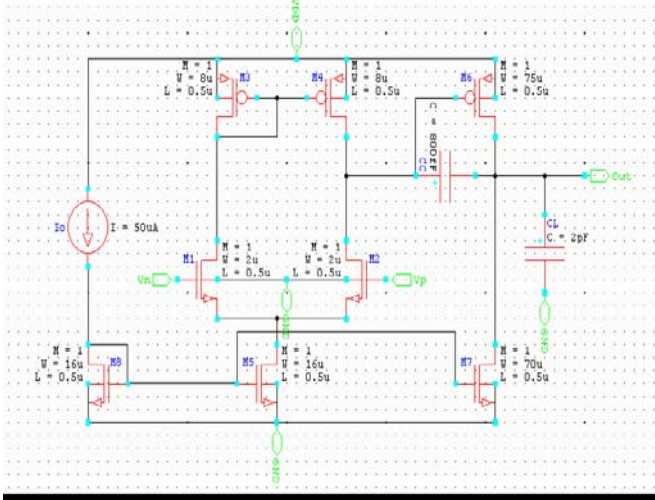


Figure.3: Schematic of Two-Stage Op-Amp

Table .2 Aspect ratio of transistors

Transistor	$S_i = (W_i/L_i)$	Ratio
M1	2µm/0.5µm	4
M2	2µm/0.5µm	4
M3	8µm/0.5µm	16
M4	8µm/0.5µm	16
M,5	16µm/0.5µm	32
M6	75µm/0.5µm	150
M7	70µm/0.5µm	140
M8	16µm/0.5µm	32

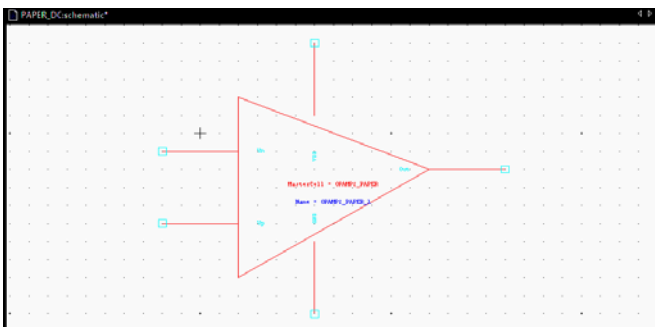


Figure.4: Symbol of Two-Stage Op-Amp

5.1 DC analysis

DC analysis is used to determine the quiescent point of the device operation. In two-stage Op-Amp, all the transistors must work in saturation. To determine that all transistors are operating in saturation or not for the entire input common mode range, DC analysis is performed. The DC analysis of Op-Amp also gives the information about the characteristic of Op-Amp i.e. trans-conductance, threshold voltage, current gain value etc.

Fig. 5 shows the set-up for DC analysis of Two-Stage Op-Amp. The minimum common mode range input supply of 1V is applied to both the input terminals.

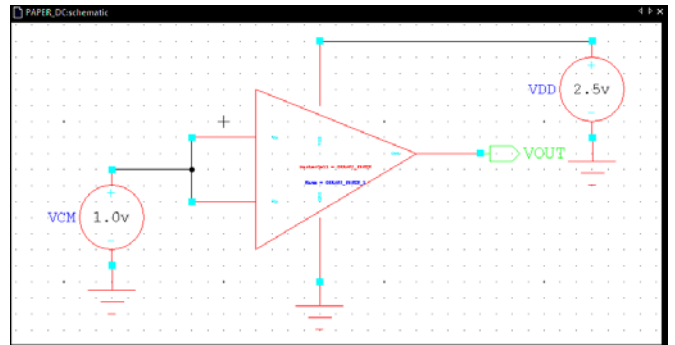


Figure.5: Set-up for DC analysis of Two-Stage Op-Amp.

5.2 AC analysis

Ac analysis is used to determine the open-loop gain, gain-bandwidth, 3-db cutoff frequency, common mode rejection ratio, power supply rejection ratio and phase margin of two-stage Op-Amp. The AC analysis gives the frequency response of the two-stage Op-Amp. Ac analysis is performed by connecting an AC source to the one of the input terminal of with the minimum dc value required to keep the transistors in the saturation region [15].

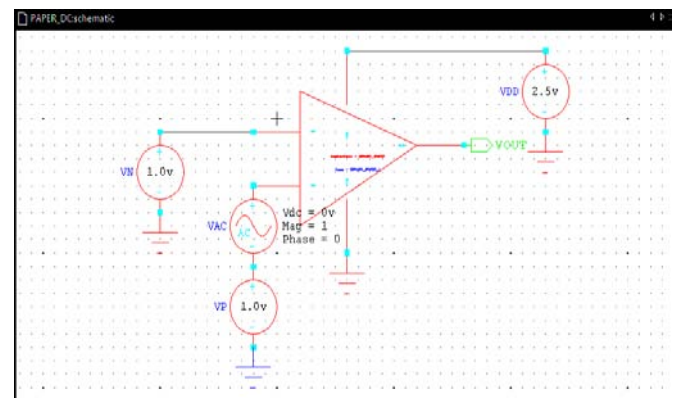


Figure. 6: Set-up for AC analysis of Two-Stage Op-Amp

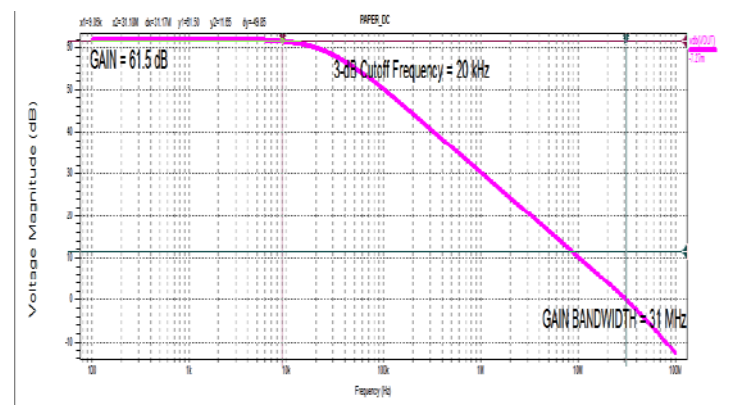


Figure. 7: Gain –frequency plot for Two-Stage Op-Amp

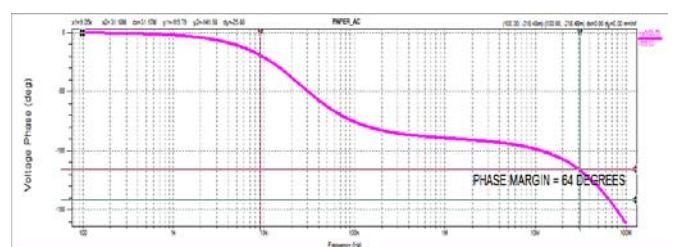


Figure.8: Phase-Frequency plot for Two-Stage Op-Amp

5.3 Transient analysis

Transient analysis gives the timing details of the device. In the case of two-stage Op-Amp, transient analysis is used to determine settling time, slew rate, output voltage swing. The transient analysis shows how fast the system or device respond to the applied input. The transient response is performed by applying sinusoidal input and pulse input [3].– [10].

5.3.1 Sinusoidal input

Transient analysis of Op-Amp using sinusoidal input is used to determine the output voltage swing.

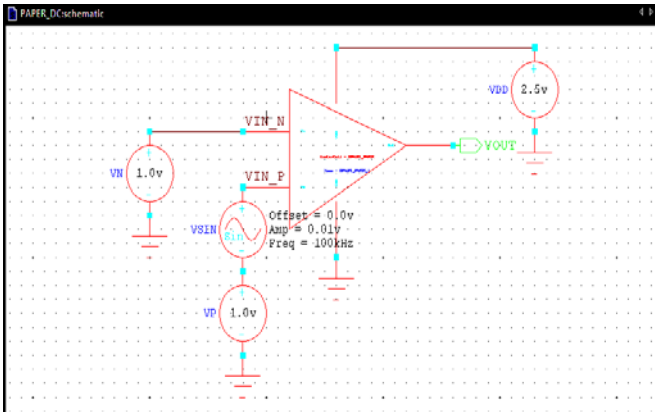


Figure .9: Set-up for Transient analysis with sinusoidal input

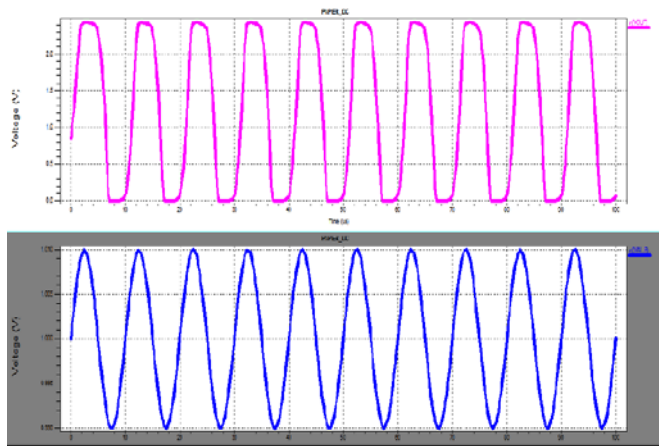


Figure. 10: Transient Analysis Output for sinusoidal input

5.3.2 Pulse input

Transient analysis of Op-Amp using Pulse input is used to determine the speed of Op-Amp. The slew rate (SR) and setting time of Op-Amp is obtained from the transient analysis using pulse input.

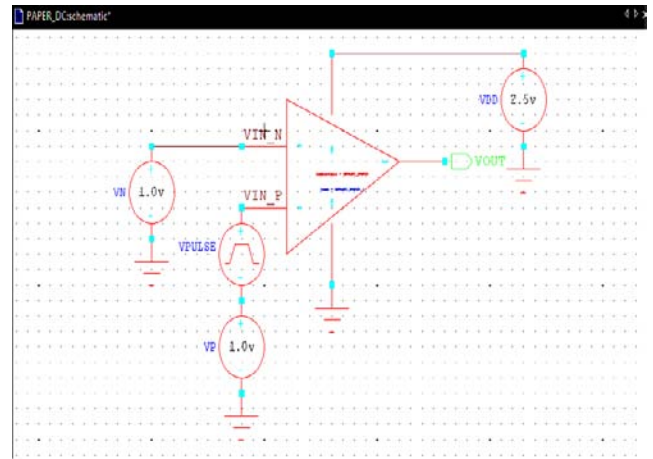


Figure. 11: set-up for Transient analysis with pulse input

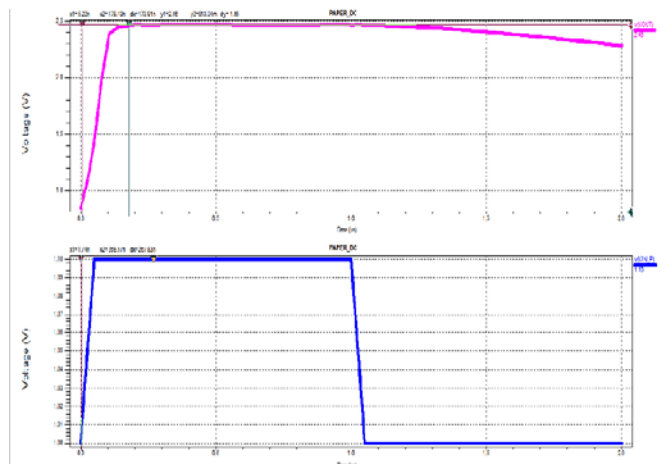


Figure .12: Transient analysis output with pulse input

Table .3 Summary of Results

S. No.	Parameter	Value
1.	Technology	0.25 μ m CMOS
2.	Supply Voltage	2.5V
3.	Current	0.328 μ A
4.	C _L	2pF
5.	C _C	800fF
6.	Open-loop gain	61.5 dB
7.	Gain-bandwidth	31 MHz
8.	3-dB cutoff frequency	20 kHz
9.	Phase Margin	64°
10.	Slew Rate	10V/ μ s
11.	Settling time	0.18 μ s
12.	Power consumption	0.82mW

6. Conclusion

From this paper, it is concluded that the design of an analog system requires the tradeoff among speed, power and other factors that characterize the performance of the system. Various applications of Op-Amp require different specifications. The different topologies of Op-Amp can be

used for different applications as per requirements. The design approach of Op-Amp can be different but the various characterizing parameters are same. So the same analysis can be performed to determine the characteristics of Op-Amp topologies.

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